Hybrid Bidirectional Multilevel Inverter Structures for Induction Motor Drive

Santhi Rama Chandran[1*]
[1*]Department of Electrical and Electronics Engineering, Srinivasa Ramunujan Center, Sastra Deemed University, Thanjavur, India

Srinivasan Anandhan[2]
[2]Department of Electronics and Communications Engineering, SASTRA Deemed University, Thanjavur, India

Abstract—Multilevel inverters performance enhancement is a major topic which has attracted the attention of most of the researchers, to evolve with newer topologies and modulation strategies. In this manuscript two novel hybrid bidirectional multilevel inverter structures which are suitable for bidirectional loads are proposed. An enhancement in the voltage levels and reduction of the component count are achieved for these newly introduced structures. Modular expansion and series cascading are suggested systems for extension of the voltage levels.The prime requirement in most of the industrial drives is a controlled output. VSI fed Induction motor drive satisfies this requirement. The Multicarrier PWM technique has been applied to the basic bidirectional seven level models and nine level model and its performance with induction motor as load has been analyzed for various modulation indices. The simulated results of the proposed structures are verified using MATLAB/SIMULINK platform. The characteristics such as stator current, rotor current speed and torque plots achieved as above model affirm that its performance is good.

Keywords—*Hybrid bidirectional Multilevel Inverter; cascading; modular expansion; Phase disposition Multicarrier Pulse width Modulation (PDMPWM); Total Harmonic distortion (THD);Induction motor drive.*

I. INTRODUCTION

The future era of power electronics is focused on energy conservation so as to attain a pollution free environment by adopting energy efficient power modulators for power conversion. Multilevel inverters have become an integral component of the power electronic system. Multilevel inverter

has been used in variety of applications which include high speed adjustable drives, Facts devices for reactive power compensation, battery powered vehicles and for grid integration [1-8].Because of its ever increasing applications the performance improvement of multilevel inverter had been most essential criteria and it attracted many researchers towards introducing newer topologies and control techniques [9-11].

In conventional inverters losses and the output voltage harmonic content were found to be too high so multilevel inverter has emerged as an alternative to address this issue and also to attain high voltage levels. The role of MLI is to synthesize a stepped waveform output voltage with better quality and lesser THD. As the number of stages maximizes, the harmonic content decreases significantly in output voltage step waveform [12].

The three major classical topologies of MLI are clamped diode [13, 14], flying capacitor [15, 16], and cascade type [17, 18]. The requirement of a large number of diodes at neutral point and neutral point voltage balance problems are the draw backs and in flying capacitor the need of many storage capacitors and capacitor voltage balancing issue were the demerits. In case of cascaded H Bridge requirement of many isolated sources has been the major drawback. Inspite of its disadvantage it is more widely used owing to its modularity and its structure is devoid of passive energy storing devices.

Increased switch count and its related gate driver circuits and protection circuit were the main disadvantages of multilevel inverters. To overcome these issues many researchers have suggested newer topologies with innovative ideas [19-22]. Many derived structures like Artificial neutral point clamped derived from NPC converter and Packed U cell converter derived from FC with component reduction has been introduced [23].

Several Hybrid topologies which combine two topologies have been emerged. Cascaded Multilevel inverter with sub multilevel inverters and modular multilevel converter were among the emerging structures which has been recently introduced [24]. Hybrid inverters mainly consist of two sub-circuits. One basic circuit generates the required positive levels and the other circuit functions as a polarity reversal circuit which is an H- bridge circuit. [25-29].

A space-vector-modulated pulse width-modulation (PWM) scheme has been suggested for the power circuit topology proposed. With this PWM scheme, a total of 64 space-vector combinations are possible, distributed over 19 space-vector locations. A further improvisation is suggested in which two two-level inverters with unequal dc-link voltages (which are in the ratio 2:1); feed an open-end winding induction motor. It has been shown that this configuration is capable of achieving four-level inversion. The total number of space-vector locations produced in this scheme is enhanced to 37. A reduction in the switching ripple is achieved with this scheme, compared to the former, as the number of constituent sectors is enhanced to 54, compared to 24 with the former. Mohammad Rezaei et al., [30] have illustrated a new cascaded switched-capacitor multilevel inverters (CSCMLIs) using two modules containing asymmetric DC sources to generate 13 levels. Dyanamina and Kakodia [31] have performed to improve the speed response; a compensating voltage component is supplemented by an amending integrator.

This manuscript is mentioned as following sections I. Introduction II. Operation of basic topology and its level expansion methods and comparison of recommended structures with other structures III. Analysis of simulation and experimental outcomes. IV. Conclusion.

II. OPERATION OF THE BASIC TOPOLOGY

The basic unit which is a seven level bi directional MLI model as referred by Samsami et al., is demonstrated [32-36] at Figure 1.

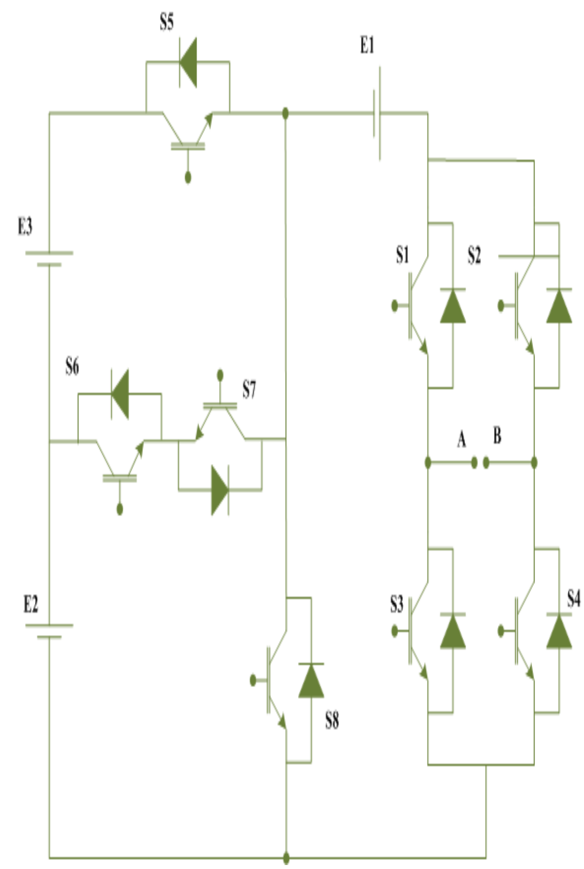

Figure 1: Seven Level bidirectional MLI

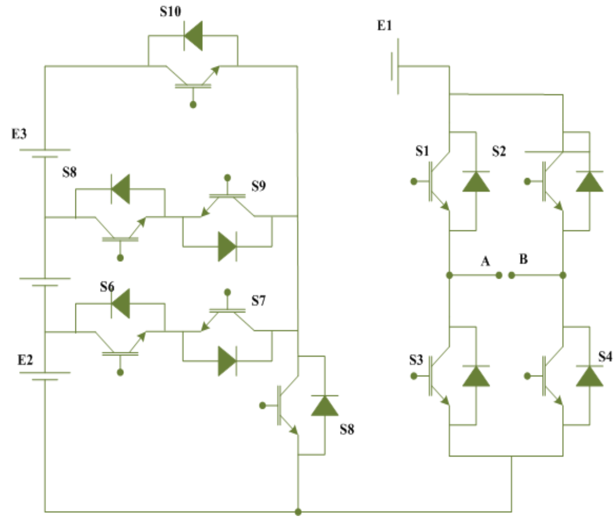

Figure 2: Nine level bidirectional MLI

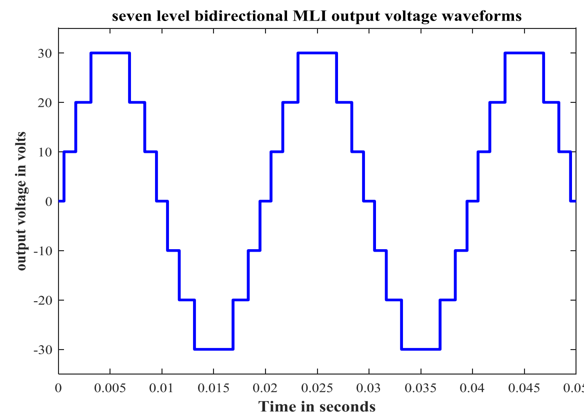

Figure 3: Output Voltage waveform of 7LBMLI

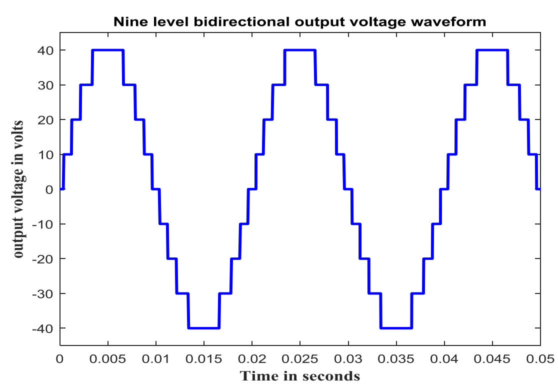

Figure 4: Output Voltage waveform of 9LBMLI

This structure is capable of supplying inductive loads with bidirectional current. The basic circuit comprises of seven IGBT switches. In that six switches are unidirectional and one switch is bidirectional. The operation of this circuit is described by a switching table as indicated in table 1 for symmetrical voltage selection.When S5 is on and S6/S7 and S8 is off it produces level 1 with E1 as output voltage. When S6 is on and S5 and S8 are off then it produces E1+E2 as output voltage. When S8 is on and S5 and S6/S7 is off it produces E1+E2+E3 as the output voltage [37-41]. An output voltage waveform for seven level circuits is shown in Figure

1.With a symmetrical voltage selection by suitable relationship of voltages the number of output stages could be extended as nine.The nine level models can also be obtained by modular expansion method by including one more voltage source and a bidirectional switch as indicated in Figure 2 [42-45] and their output voltage waveform is demonstrated at Figure 3 and 4.

Table 1: Switching Sequence of basic 7LBMLI

S1	S2	S3	S4	S5	S6/S7	S8	Load Voltage $V_{AB}(t)$
1	1	0	0	0	0	0	0
1	0	1	0	1	0	0	vdc
1	0	1	0	0	1	0	2Vdc
1	0	1	0	0	0	1	3Vdc
0	0	1	1	0	0	0	0
0	1	0	1	1	0	0	-Vdc
0	1	0	1	0	1	0	-2Vdc
0	1	0	1	0	0	1	-3Vdc

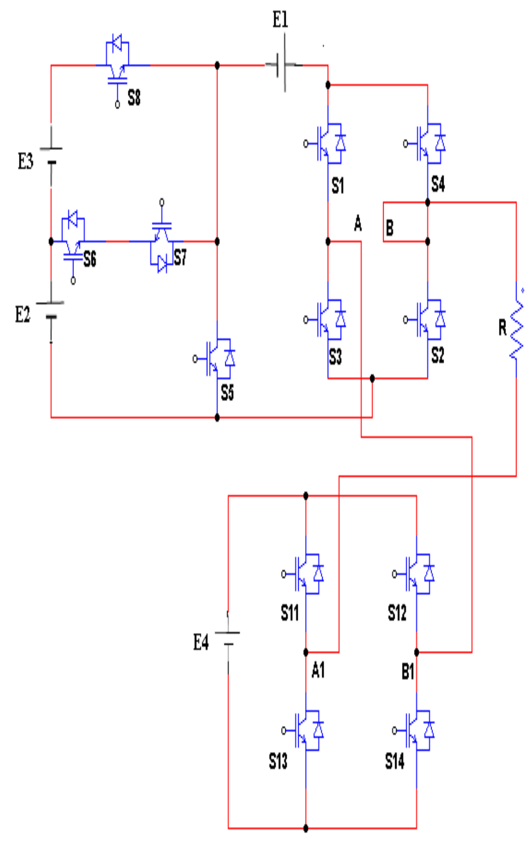

Figure 5: Proposed hybrid structure 1 (7L basic unit cascaded with H-Bridge circuit)

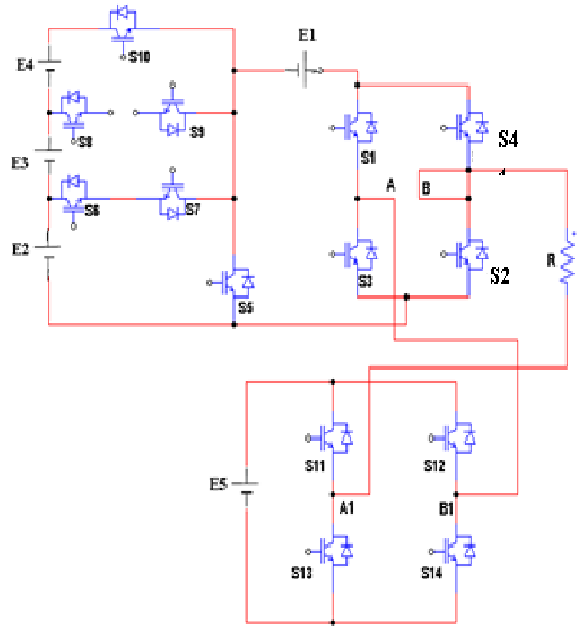

Figure 6: Proposed hybrid structure 2(9L basic unit cascaded with H-Bridge circuit)

2.1. Level extension methods

Modular expansion, normal and staircase layer are process of increasing the output levels. Table 2 shows the component requirement and source requirement for specific levels using modular expansion.

Table 2: Modular expansion method

S.No	No of unidirectional switches	No of Bidirectional switches	No of levels(N)V0=2*M+1	No of Sources(M)
1	6	1	7	3
2	6	2	9	4
3	6	3	11	5
4	6	4	13	6

2.1.1. Cascading basic units with H-Bridge circuit

By cascading the basic 7L unit with H-Bridge circuit with E1=E2=E3=1 Vdc and E4 voltage as 7vdc as illustrated in Figure 5 is able to produce 21 level output. If a nine level circuit is cascaded with H-bridge circuit with E1=E2=E3=1Vdc and E4 voltage as 9Vdc it is able to produce 27 level output voltage as depicted in Figure 6.

Table 3: Extension of levels by cascading basic circuit

S.No	Various Cascading methods using symmetric structures	DC sources ratio	No of unidirectional switches	No of Bidirectional switches	No of levels(N)	No of Sources(M)
1	Basic unit and one H bridge	01:07	10	1	21	4
2	basic unit and two H bridges	01:07:07	14	1	35	5

3	basic 1and unit 2	unit basic	01:0 7	12	2	49	6

2.1.2.Cascading of basic unit with another basic unit

When 7L basic unit is cascaded with another unit, both has voltages as symmetric with E1=E2=E3 =Vdc it produces thirteen level output. If asymmetric method is chosen still more increase in levels are achieved.When the first 7L basic unit is having E1=E2=E3 =Vdc and the cascading unit is having E4=E5=E6=7Vdc as illustrated in Figure 7 is probable for creating 49 Level output wave form. As the voltage levels increase the harmonic content in output voltage waveform reduced. Some of the ways to cascade with the base circuit for maximizing the number of stages is represented in Table 3 and component comparison with CHB MLI is suggested on table 4.

Table 4: Component Comparison of the 49L HBMLI with CHB Symmetrical MLI

Parameters	CHB symmetrical	Proposed bidirectional topology
No of H-Bridges	24	0 (instead it needs another basic unit in series)
No of Dc sources	24	6
No of Switches	96	16
No of output Levels	49	49

2.3.49L Hybrid proposed structure derived using cascading of two similar units

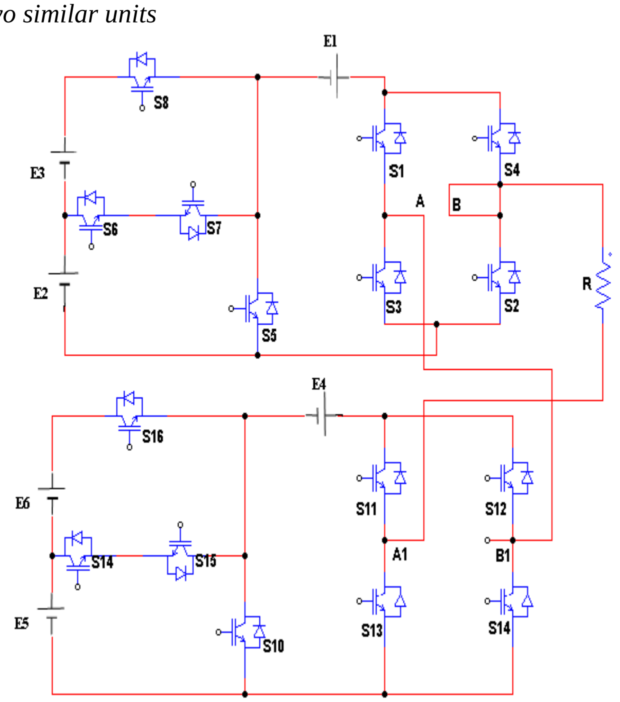

Figure 7: proposed hybrid structure by cascading basic unitswitch dc sources ratio (1:7)

3. Simulation and experimental results and analysis for the hybrid structures

The output voltage waveform for 21L circuit obtained by cascading a single phase 7L basic unit cascaded with H-Bridge circuit with RL load with R=100Ω and L=50mH is indicated in Figure 8. The THD content on output voltage waveform found to be 3.90 as depicted on Figure 9.

An output voltage waveform for 49L circuit obtained by cascading a single phase 7L basic unit1with similar 7L basic unit2 in asymmetric topology with DC voltage distribution ratio of the sources in the ratio 1:7 with R load with R L load are illustrated on Figure 10 and Figure 11. An output obtained from the basic unit and the cascaded units are shown in Figure 12 and Figure 13. The FFT analysis is demonstrated on Figure 14 and THD content on output voltage waveform is found to be 2.88.

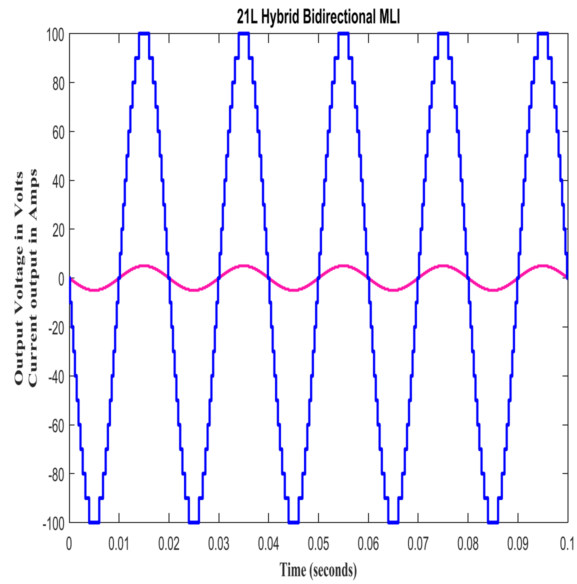

Figure 8: 21Level hybrid BMLI output voltage

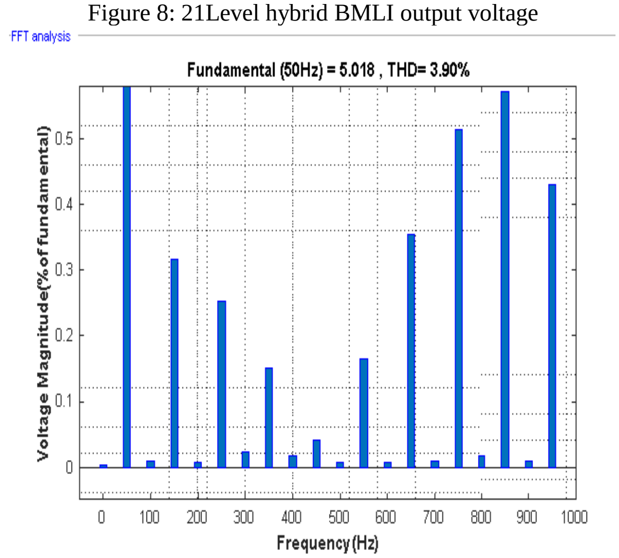

Figure 9: Voltage harmonic Spectrum of 21L hybridBMLIcurrent waveform

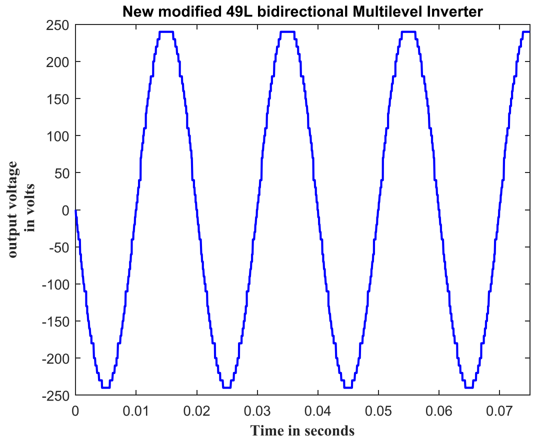

Figure 10: Output voltage waveform of 49L HBMI

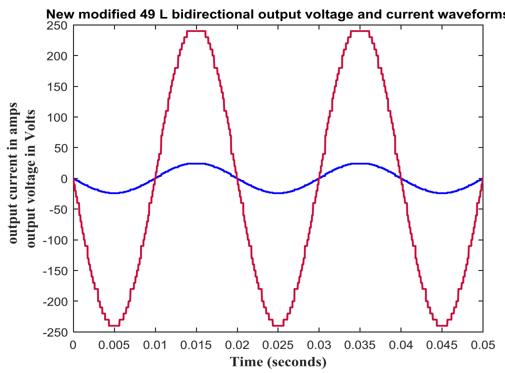

Figure 11: Output current waveform of 49L HBMLI

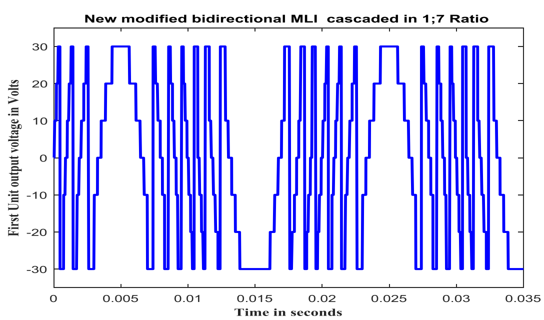

Figure 12:Output voltage waveform of basic unit1

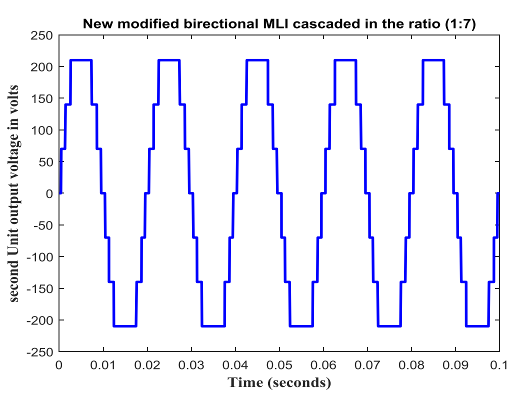

Figure 13:Output voltage waveform of basic unit2

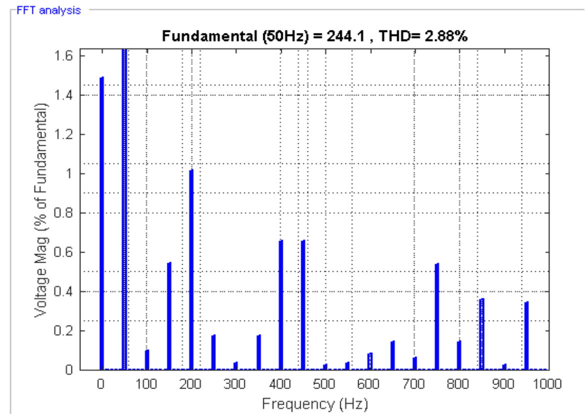

Figure 14: Voltage harmonic spectrum of 49L HBMI

The 21L HBMLI is tested using three phase induction motor model available in MALAB Simulink as the load and its performance characteristics like stator current, rotor current, speed ,torque are analyzed. The twenty-one level three phase bidirectional MLI fed induction motor model diagram using MATLAB Simulink is illustrated by Figure 15. The performance characteristics of the 21 level HBMLI like speed, stator current, torque, rotor current are presented in Figure 16, Figure 17 and Figure 19 and the phase voltages are shown in Figure 18.

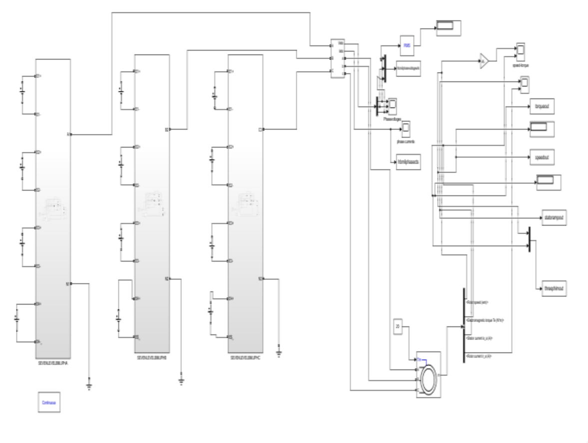

Figure 15: Twenty one levels HBMLI fed Induction motor drive

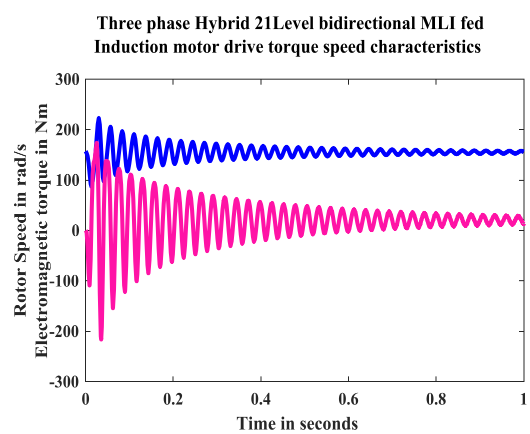

Figure 16: Speed, torque characteristics of twenty one level HBMLI

DOI: 10.46300/9101.2022.16.21 Volume 16, 2022

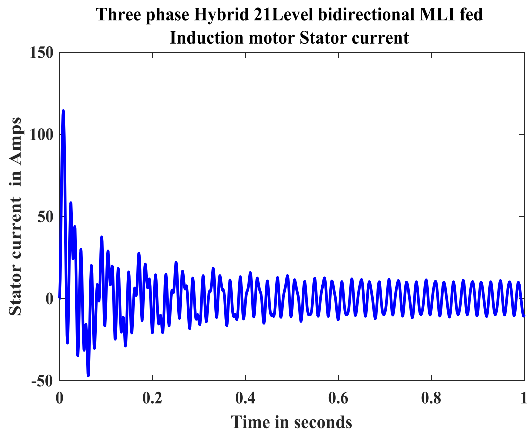

Figure 17: Stator current characteristics of Twenty-one level HBMLI

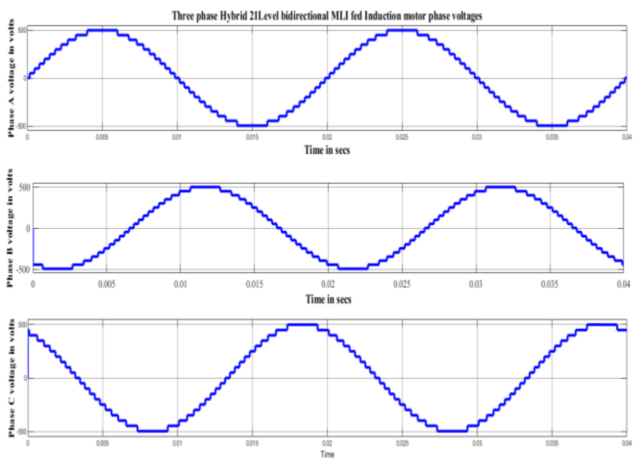

Figure 18:Twenty-one HBMLI phase voltages

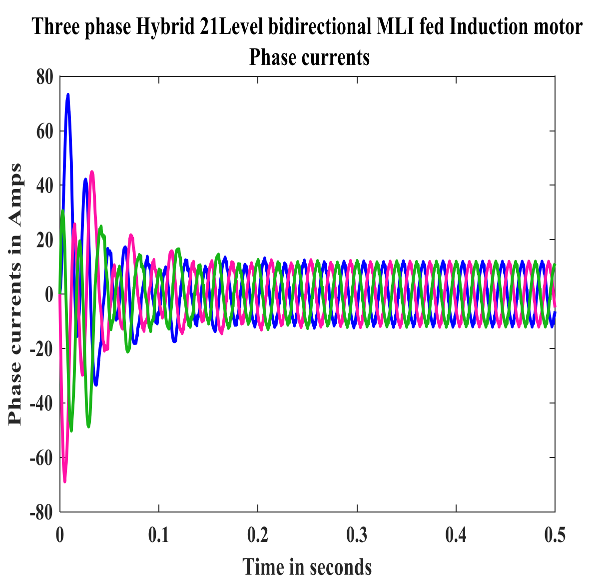

Figure 19: 21 level Three phase HBMLI fed Induction motor drive Phase currents

Table 5: Performance of Three phase 9-level BMLI fed Induction motor at No load

Modulating Wave for PDPWM	M.I	Three Phase Induction Motor fed with 9-Level CHBMLI		
		V line in Volts	%THD	V_{AN} in Volts
Sine wave	1	493.3	11.73	285.5
	0.8	396	14,3	229.7
	0.6	301	22.07	174,6
	0.4	208	35.63	121.2

Simulink model three phase induction motor (asynchronous motor) of 5.4 H.P, 400V, 50 Hz and 1430 RPM rated speed has been chosen from Simulink library. PDPWM control technique is applied by selecting modulation index as 1.0 and switching frequency of IGBT is selected 1 kHz and that of modulating wave is 50Hz respectively. Even though various speed control methods are available for induction motor v/f speed control technique is the mostly preferred one due to its characteristics such as good transient and dynamic performance. It also provides good speed control range and it is easier to implement

For authenticating the efficiency of 7L BMLI, the induction motor is worked in the range with a standard V / F mode (0 <mi <1) with varying modulation indexes and its readings are tabulated in Table 5.

Seven level BMLIs in dissimilar modulation codes (0.4, 0.6, 0.8 and 1.0) are recommended on Figure 20-23.The variation of modulation index modifies the number of stages.The stator currents are nearly sinusoidal for all cases of M.I values and the stator current for M.I=1 is shown in Figure 24.

Table 6: Performance of Three phase 7-level BMLI fed Induction motor at No load

Modulating Wave for PDPWM	M.I	Three Phase Induction Motor fed with 7-Level HBMLI		
		V line in Volts	%THD	V_{AN} in Volts
Sine wave	1	371.8	15.06	215.7
	0.8	301	22.10	174.6
	0.6	230.1	29.9	134.2
	0.4	157.3	38.13	92.87

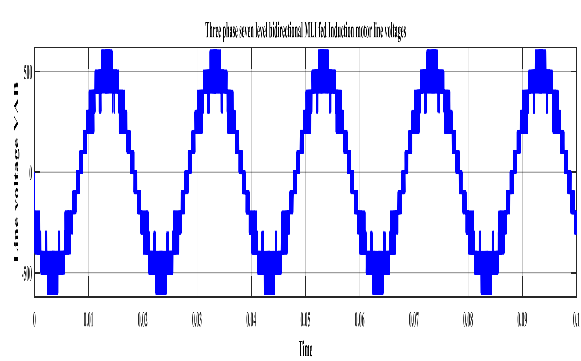

Figure 20: Line voltage VAB for M.I=1 using PDPWM at switching frequency as 1kHz

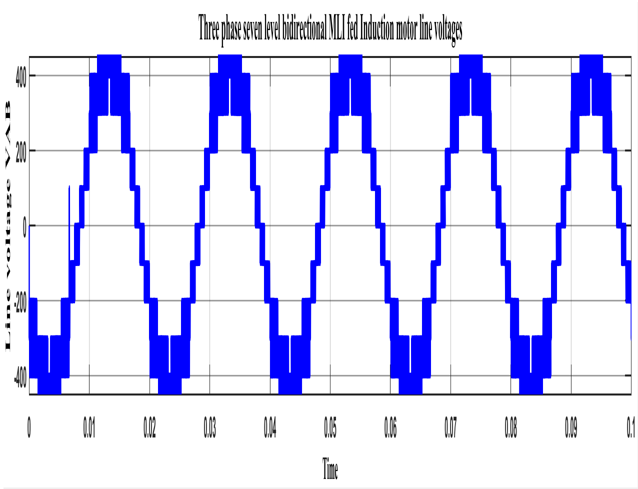

Figure 21: Line voltage VAB for M.I=0.8 using PDPWM at switching frequency as 1kHz

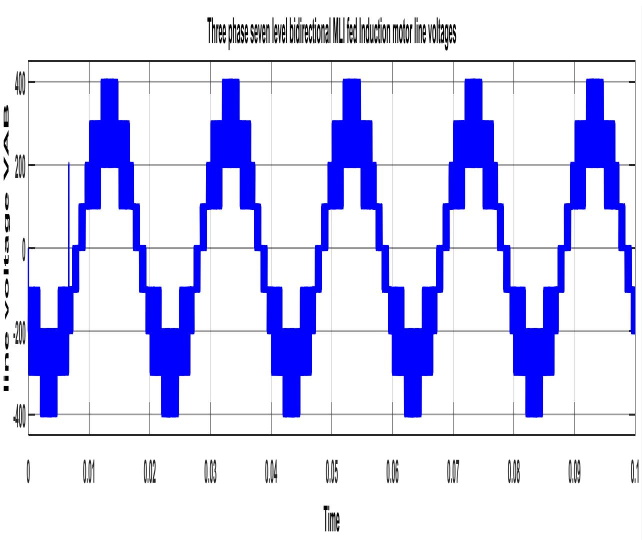

Figure 22: Line voltage VAB for M.I=0.6 using PDPWM at switching frequency as 1kHz

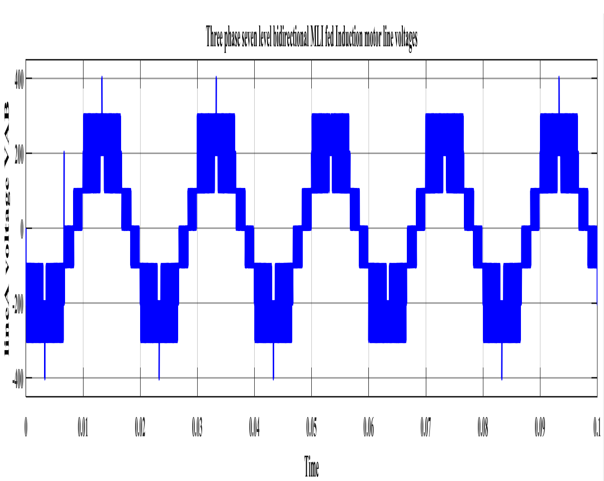

Figure 23: Line voltage VAB for M.I=0.6 using PDPWM at switching frequency as 1 kHz

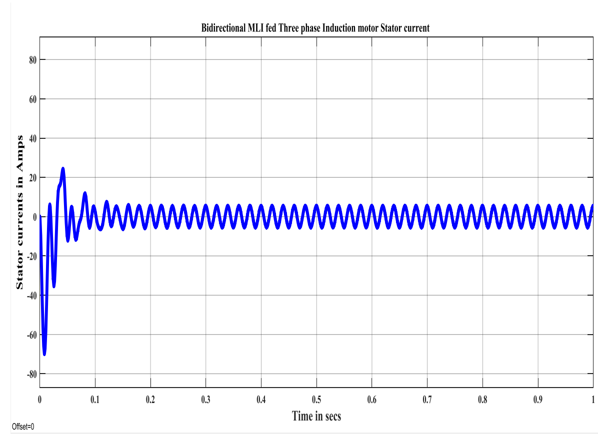

Figure 24: Stator current of BMLI fed induction motor when M.I=1

The performance of the 9 BMLI has been verified by operating the induction motor by varying the modulation index in the range (0<M.I <1) with standard V/f mode and its readings are tabulated in Table.6. The line and phase voltage of nine stages BMLI are demonstrated on Figure 25 and Figure 26.

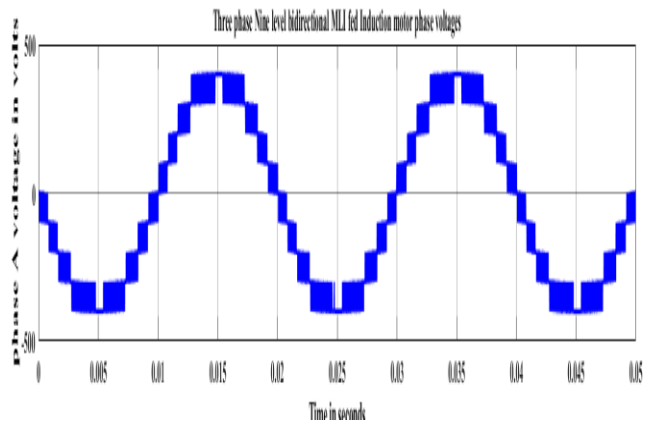

Figure 25: Phase voltage Van with M.I=1 and switching frequency 1 kHz using PDPWM technique

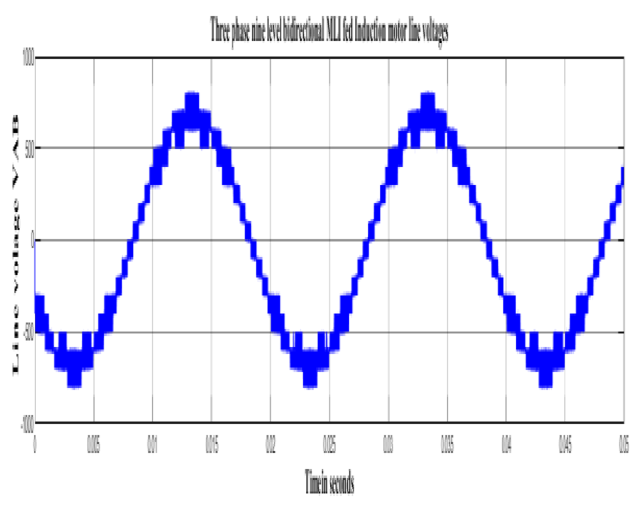

Figure 26: Line voltage V_{AB} with M.I=1 and switching frequency 1 kHz using PDPWM technique

Table 7: Efficiency for various topologies

Various topologies	Efficiency obtained (%)
Proposed technique	99.003
H-bridge topology	80.343
Flying capacitor topology	75.603
Neutral point clamped (NPC) topology	55.893

Table 7 explains the efficiency of the conventional and proposed topology. The proposed topology affirms the best result over the conventional topology. The efficiency values of the proposed topology are 99.003%.

IV. CONCLUSION

In this manuscript two novel hybrid bidirectional MLI configurations are proposed. The simulated results are obtained for 21 L and 27 L for the proposed structures by series cascading with level doubling network. The simulated results are verified for 49L and 81L output, which are synthesized using series cascading method with two similar basic units. All these hybrid BMLI structures produced output with lesser voltage harmonic content. The simulated results of the three phase 21 LHBMLIMATLAB SIMULINK model with induction motor as the load is verified. Certainly, this hybrid BMLI structures with increased output voltage levels and minimized THD would be well suited for medium powered AC drive applications.

REFERENCES

[1] J. Lee, A. Rizvi, F. Lin, J. Min, B. Hartaigh and D. Han. 2016. "Fractional Flow Reserve Measurement by Computed Tomography: An Alternative to the Stress Test", *Interventional Cardiology Review*, vol.11, no.2, pp.105, Available: 10.15420/icr.2016:1:2.

[2] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo and M. Prats. 2008. "The age of multilevel converters arrives", *IEEE Industrial Electronics Magazine*, vol.2, no.2 pp.28-39, Available: 10.1109/mie.2008.923519.

[3] D. Abbott. 2010. "Keeping the Energy Debate Clean: How Do We Supply the World's Energy Needs"?, *Proceedings of the IEEE*, vol.98, no. 1, pp.42-66, Available:10.1109/jproc.2009.2035162.

[4] X. Yu, C. Cecati, T. Dillon and M. Simões, 2011. "The New Frontier of Smart Grids", *IEEE Industrial Electronics Magazine*, vol.5, no.3, pp.49-63, Available:10.1109/mie.2011.942176.

[5] S. Mythili, K. Thiyagarajah, P. Rajesh and Shajin FH. 2020. "Ideal position and size selection of unified power flow controllers (UPFCs) to upgrade the dynamic stability of systems: an antlion optimiser and invasive weed optimisation algorithm". *HKIE Trans*, vol.27, no.1, pp.25-37,

[6] P. Rajesh, F. A. Shajin, 2020. "Multi-Objective Hybrid Algorithm for Planning Electrical Distribution System", *European Journal of Electrical Engineering*, vol.22, no.1, pp.224-509,

[7] FH. Shajin, P. Rajesh. 2020. "Trusted secure geographic routing protocol: outsider attack detection in mobile ad hoc networks by adopting trusted secure geographic routing protocol". *International Journal of Pervasive Computing and Communications*.

[8] MK. Thota, FH. Shajin and P. Rajesh. 2020. "Survey on software defect prediction techniques". *International Journal of Applied Science and Engineering*. Vol.17, no.4, pp.331-44,

[9] Y. Liao and C. 2011. Lai. "Newly-Constructed Simplified Single-Phase Multistring Multilevel Inverter Topology for Distributed Energy Resources", *IEEE Transactions on Power Electronics*, vol.26, no.9 pp.2386-2392, Available: 10.1109/tpel.2011.2157526.

[10] K. Gupta and S. Jain. 2012. "Topology for multilevel inverters to attain maximum number of levels from given DC sources", *IET Power Electronics*, vol.5, no. 4, pp.435, Available: 10.1049/iet-pel.2011.0178.

[11] N. Abd Rahim, M. Mohamad Elias and W. Hew. 2012. "Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter with New Method of Capacitor Voltage Balancing", *IEEE Transactions on Industrial Electronics*, vol.60, no.8, pp.2943-56.Available: 10.1109/tie.2012.2200213.

[12] J.S. Lai and F.Z. Peng, 1996. "Multilevel converters-a new breed of power converters", *IEEE Transactions on Industry Applications*, vol.32, no.3 pp.509-517, Available: 10.1109/28.502161.

[13] L. Tolbert, J. Chiasson, Z. Du and K. McKenzie. 2005. "Elimination of Harmonics in a Multilevel Converter WithNonequal DC Sources", *IEEE Transactions on Industry Application*s, vol.41, pp.75-82, Available: 10.1109/tia.2004.841162.

[14] A. Nabae, I. Takahashi and H. Akagi. 1981. "A New Neutral-Point-Clamped PWM Inverter", *IEEE Transactions on Industry Applications*, pp.518-523, Available: 10.1109/tia.1981.4503992.

[15] Nabae, I. Takahashi and H. Akagi. 1981. A New Neutral-Point-Clamped PWM Inverter, *IEEE Transactions on Industry Applications*, vol.5, pp.518-523, Available: 10.1109/tia.1981.4503992.

[16] T. Meynard and H. Foch. 1992. "Multi-Level Choppers for High Voltage Applications", *EPE Journal*, vol.2, no.1, pp.45-50, Available: 10.1080/09398368.1992.11463285.

[17] J. Myers. 1997. The United States patent and trademark office internet home pages", *World Patent Information*, vol.19, pp.77-78, Available: 10.1016/s0172-2190(97)82780-9.

[18] P. Hammond. 1997."A new approach to enhance power quality for medium voltage AC drives", *IEEE Transactions on Industry Applications*, vol.33, no.1, pp.202-208,Available: 10.1109/28.567113.

[19] T.L.Wherry.1993."Survey of missing patents at the United States patent and trademark office", *World Patent Information*, vol.15, no.3, pp.182, Available: 10.1016/0172-2190(93)90019-s.

[20] P. Chaturvedi, S. Jain and P. Agrawal. 2011. "A simple carrier-based neutral point potential regulator for three-level diode clamped inverter", *International Journal of*

Power Electronics, vol.3, no.1, pp.1-25, Available: 10.1504/ijpelec.2011.037331.

[21] Y. Liu and F. Luo. 2006. "Multilevel inverter with the ability of self-voltage balancing", *IEE Proceedings - Electric Power Applications*, vol. 153, no.1, pp.105-115, Available: 10.1049/ip-epa:20050192.

[22] S. De, D. Banerjee, K. Siva kumar, K. Gopakumar, R. Ramchand and C. Patel. 2011. "Multilevel inverters for low-power application", *IET Power Electronics*, vol.4, no.4, pp.384, Available: 10.1049/iet-pel.2010.0027.

[23] Hua, C. Wu and C. Chuang. 2009. "A novel dc voltage charge balance control for cascaded inverters", *IET Power Electronics*, vol.2, no.2, pp.147-155, Available: 10.1049/iet-pel:20080025.

[24] K. Gupta, A. Ranjan, P. Bhatnagar, L. Sahu and S. Jain. 2016. "Multilevel Inverter Topologies With Reduced Device Count: A Review", *IEEE Transactions on Power Electronics*, vol.31, no.1 pp.135-151, Available: 10.1109/tpel.2015.2405012.

[25] J. Venkataramanaiah, Y. Suresh and A. Panda. 2018. "Design and Development of a Novel 19-Level Inverter Using an Effective Fundamental Switching Strategy", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol.6, no.4, pp.1903-1911, Available:10.1109/jestpe.2017.2776294.

[26] Y. Suresh, J. Venkataramanaiah, A. Panda, C. Dhanamjayulu and P. Venugopal. 2017. "Investigation on cascade multilevel inverter with symmetric, asymmetric, hybrid and multi-cell configurations", *Ain Shams Engineering Journal*, vol.8, no.2, pp.263-276, Available: 10.1016/j.asej.2016.09.006.

[27] S. Daher, J. Schmid and F. Luiz Marcelo Antunes. 2007. "High Performance Inverter For Renewable Energy Systems", *Eletrônica de Potência*, vol.12, no.1, pp.253-260, Available:10.18618/rep.2007.3.25326.

[28] E. Najafi and A. Yatim. 2012. "Design and Implementation of a New Multilevel Inverter Topology", *IEEE Transactions on Industrial Electronics*, vol.59, no.11, pp.4148-4154, Available: 10.1109/tie.2011.2176691.

[29] R. Alishah, D. Nazarpour, S. Hosseini and M. Sabahi. 2014. "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels", *IET Power Electronics*, vol.7, no.1, pp.96-104, Available: 10.1049/iet-pel.2013.0156.

[30] M. Rezaei, M. Nayeripour, J. Hu, S. Band, A. Mosavi and M. Khooban, 2022. "A New Hybrid Cascaded Switched-Capacitor Reduced Switch Multilevel Inverter for Renewable Sources and Domestic Loads", *IEEE Access*, vol. 10, pp. 14157-14183, Available: 10.1109/access.2022.3146256.

[31] G. Dyanamina and S. Kakodia, 2021. "Adaptive neuro fuzzy inference system based decoupled control for neutral point clamped multi level inverter fed induction motor drive", *Chinese Journal of Electrical Engineering*, vol. 7, no. 2, pp. 70-82, Available:10.23919/cjee.2021.000017

[32] Y. Liao and C. Lai. 2011. "Newly-Constructed Simplified Single-Phase Multistring Multilevel Inverter Topology for Distributed Energy Resources", *IEEE Transactions on Power Electronics*, vol.26, no.9, pp.2386-2392, Available: 10.1109/tpel.2011.2157526.

[33] M. Calais, V. Agelidis and M. Dymond, 2001."A cascaded inverter for transformerless single-phase grid-connected photovoltaic systems", *Renewable Energy*, vol.22, no.1-3, pp.255-262, Available: 10.1016/s0960-1481(00)00069-0.

[34] G. Su. 2005. "Multilevel DC-Link Inverter", *IEEE Transactions on Industry Applications*, vol.41,no.3 pp.848-854, Available: 10.1109/tia.2005.847306.

[35] E. Babaei. 2008. "A Cascade Multilevel Converter Topology With Reduced Number of Switches", *IEEE Transactions on Power Electronics*, vol.23, no.6, pp.2657-2664, Available: 10.1109/tpel.2008.2005192.

[36] J. Ebrahimi, E. Babaei and G. Gharehpetian. 2012. "A New Multilevel Converter Topology With Reduced Number of Power Electronic Component", *IEEE Transactions on Industrial Electronics*, vol.59, no.2, pp.655-667, Available: 10.1109/tie.2011.2151813.

[37] R. Samanbakhsh and A. Taheri. 2016. "Reduction of Power Electronic Components in Multilevel Converters Using New Switched Capacitor-Diode Structure", *IEEE Transactions on Industrial Electronics*, vol.63, no.11, pp.7204-7214, Available: 10.1109/tie.2016.2569059.

[38] E. Villanueva, P. Correa, J. Rodriguez and M. Pacas. 2009. "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems", *IEEE Transactions on Industrial Electronics*, vol.56, no.11, pp.4399-4406, Available: 10.1109/tie.2009.2029579.

[39] R. ShalchiAlishah, D. Nazarpour, S. Hosseini and M. Sabahi. 2015. "Reduction of Power Electronic Elements in Multilevel Converters Using a New Cascade Structure", *IEEE Transactions on Industrial Electronics*, vol.62, no.1, pp.256-269, Available: 10.1109/tie.2014.2331012.

[40] E. Babaei, M. FarhadiKangarlu and M. Hosseinzadeh. 2013. "Asymmetrical multilevel converter topology with reduced number of components", *IET Power Electronics*, vol.6, no.6, pp.1188-1196, Available: 10.1049/iet-pel.2012.0497.

[41] H. Samsami, A. Taheri and R. Samanbakhsh. 2017. "New bidirectional multilevel inverter topology with staircase cascading for symmetric and asymmetric structures", *IET Power Electronics*, vol.10, no.11, pp.1315-1323, Available: 10.1049/iet-pel.2016.0956.

[42] R. Raushan, B. Mahato and K. Jana. 2016. Comprehensive analysis of a novel three-phase multilevel inverter with minimum number of switches, *IET Power Electronics*, vol.9, no.8, pp.1600-1607, Available: 10.1049/iet-pel.2015.0682.

[43] J. Rodriguez, S. Bernet, B. Wu, J. Pontt and S. Kouro. 2007. "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives", *IEEE Transactions on Industrial Electronics*, vo.54, no.6, pp.2930-2945, Available: 10.1109/tie.2007.907044.

[44] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L.G. Franquelo, B. Wu, J. Rodriguez, M.A. Pérez, and J.I. Leon, 2010. "Recent Advances and Industrial

DOI: 10.46300/9101.2022.16.21 Volume 16, 2022

Applications of Multilevel Converters, *IEEE Transactions on Industrial Electronics*, vol.57, no.8, pp.2553-2580, Available: 10.1109/tie.2010.2049719.

[45] D.McGrath and D.Holmes. 2002. “Multicarrier PWM strategies for multilevel inverters”, *IEEE Transactions on Industrial Electronics*, vol.49, no.4, pp.858-867, Available: 10.1109/tie.2002.801073.