INTERNATIONAL JOURNAL OF CIRCUITS, SYSTEMS AND SIGNAL PROCESSING
DOI: 10.46300/9106.2022.16.137 Volume 16, 2022

High Precision Low Input Voltage of 65nm CMOS Rectifier for Energy Harvesting using Threshold Voltage Minimization in Telemedicine Embedded System

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Received: May 17, 2022. Revised: August 11, 2022. Accepted: September 14, 2022. Published: October 7, 2022.

Abstract - **Telemedicine applications run at very low input voltages, necessitating the use of Great Precision Rectifier with high sensitivity to function at low input voltages. In this study, we used a 65 nm CMOS rectifier to achieve a 0.2V input voltage for Energy Harvesting Telemedicine application. The suggested rectifier, which has two-stage structure and operates at frequency of 2.4GHz, has been found to perform better in cases where the minimum operating voltage is lower than previously published papers, and the rectifier can operate over a wide range of low input voltage amplitudes. Full-Wave Fully gate cross-coupled Rectifiers (FWFR) CMOS Rectifier Efficiency at Freq of 2.4 GHz: With an input voltage amplitude of 2V, the minimum and maximum output voltages are 0.49V and 1.997V, respectively, with a peak VCE of 99.85 percent and a peak PCE of 46.86 percent. This enables the suggested rectifier to be used in a variety of vibration energy collecting systems, including electrostatic, electromagnetic, and piezoelectric energy harvesters. The proposed rectifier, which is built at 2.4GHz and has a two-stage structure, performs better in the event of low input voltage amplitude and has lower minimum operation voltage than previously published papers. Full-wave fully gate cross-coupled rectifiers (FWFR) CMOS Rectifier Performance Summary at Freq of 2.4 GHz: With a 2V input voltage amplitude, the minimum and maximum output voltages are 0.49V and 1.997V, respectively, with a maximum VCE of 99.85% and a maximum PCE of 46.86%.**

Keywords__ High Precision Rectifier, Wide-Band Active Rectifier, Energy Harvesting, Embedded system, IoT Telemedicine System, Threshold voltage minimization, Differential drive CMOS rectifier, Full-wave fully gate cross-coupled rectifiers (FWFR).

I. INTRODUCTION

A. Implantable Medical Device IMD Applications :
Implantable medical devices, IMD, are increasingly being used to improve the medical outcomes of patients. Therefore, implantable medical devices (IMDs) are typically used to monitor and treat a variety of medical conditions. Today, wireless modules are an important part of many modern IMDs. Therefore, doctors can use the device programmer wirelessly to configure IMD parameters. However, such wireless technologies expose IMD to security attacks. Therefore, security and privacy issues are urgent design issues in telemedicine embedded systems.

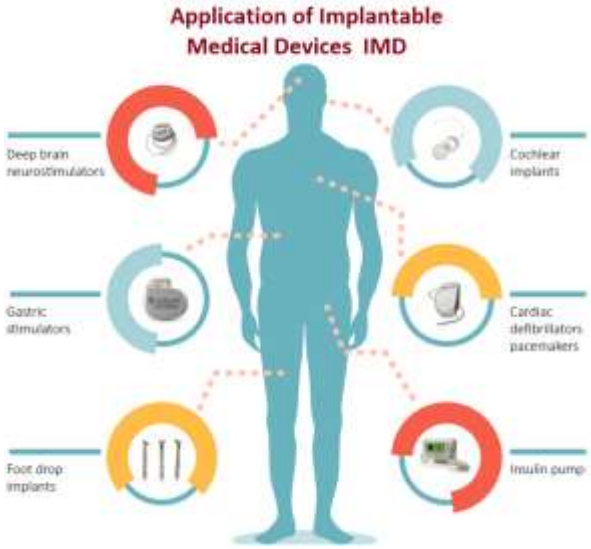

Figure 1a. Implantable Medical Device IMD Application[1]

B. Challenges for Implantable Medical Devices IMDs

designers have already considered safety, reliability, complexity, power consumption, and cost. but, current studies has proven that designers have to additionally don't forget protection and facts privateness to defend sufferers from acts of robbery or malice, in particular as clinical era turns into more and more related to different structures through wi-fi communications or Internet. As developments in energy efficiency, sensing, wi-fi structures and bio-interfaces make viable new and advanced IMDs, additionally they underscore the significance of knowledge and addressing protection and privateness issues in an more and more related global as proven in Fig.2 . Energy harvesting structures has turn out to be the maximum crucial troubles because of the vulnerable sign from the human body.

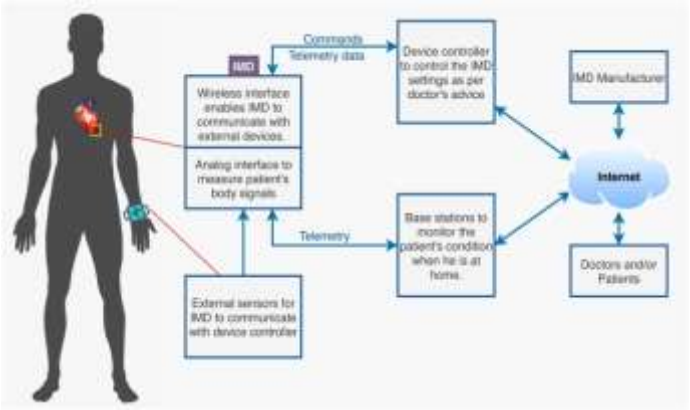

Figure 1b. Telemetry, Security and privacy concerns in IMD

C. Energy Harvesting and Powering of IMD

Due to weak coupling, skin absorption, and a narrow bandwidth passage, wireless power transfer technology has a very low power transfer efficacy. Therefore, it is vital to utilize an effective rectification mechanism to handle the power received from the coupling coil's secondary winding. Telemedicine Embedded systems sometimes receive low voltage levels of vital signs in the human body to diagnose the patient's health. Therefore, it is necessary to design a low threshold voltage rectifier that can detect low input voltage. Which parameter affects the threshold voltage? In Figure.2, the threshold voltage depends on the following parameters: 1. Gate material, 2. Gate insulator, 3. Gate insulation thickness, 4. Channel doping, 5. Impurities on the Silicon Insulator interface, 6. Voltage between source and board, 7. temperature.

An important value that characterizes MOSFET transistors is the threshold voltage value. Depending on the type of MOSFET, the threshold voltage value can be positive or negative. This value can be controlled during the MOSFET transistor manufacturing process. The effects of channel length L, drain (source) region depth xj, consuming-source voltage (VDS) on voltage term ΔVto are shown in Figures 1, 2, and 3 [2].

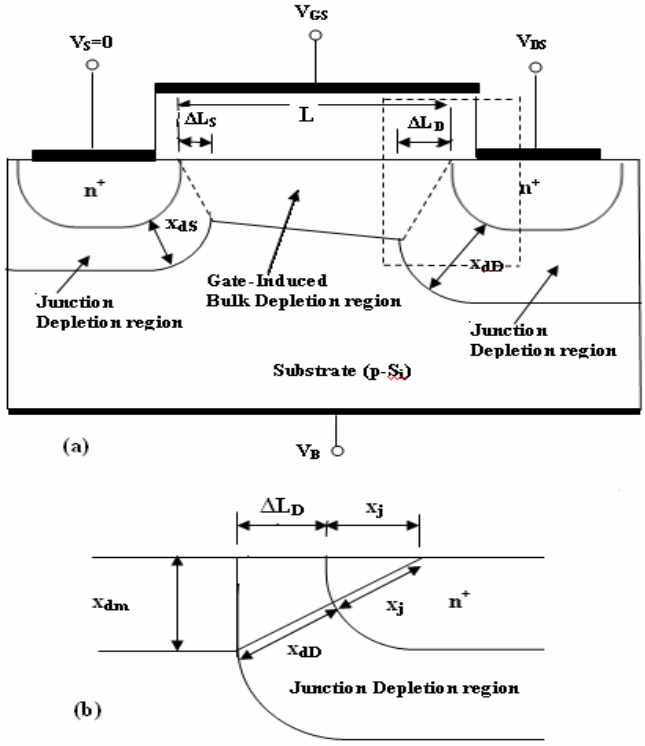

Figure 2a. Simplified geometry of MOSFET channel region, with gate-induced bulk depletion region and pn-junction depletion region. (b) Close-up view of drain diffusion edge [1]

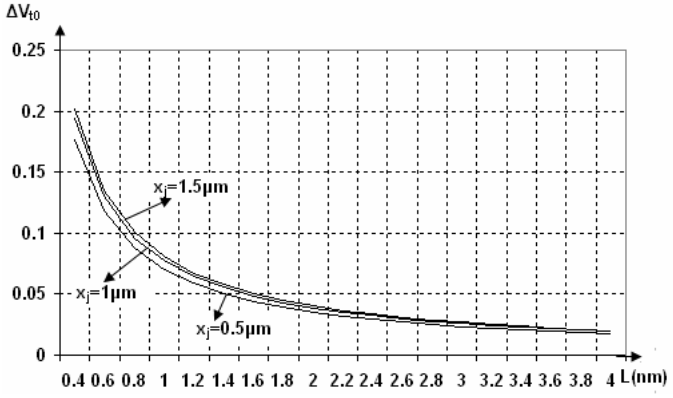

Figure 2c. Dependence of ΔVto on length L for parametric values of depth xj, when NA = 1016 cm-3, ND = 1018 cm-3, tox = 20 nm and VDS = 0V[2].

Based on obtained values which might be represented in Fig.1, Fig.2 and Fig.3, for L ≈ xj the ΔVt0 can have an impact on in discount of the edge voltage Vt0. While if L >> xj the ΔVto isn't massive, the NMOS is

described as long-channel device. Booming cost of bounds NA and xj can have small have an impact on in time period of the edge voltage ΔVto. The VDS voltage can have massive have an impact on withinside the time period ΔVto, which ends up in large cost for better cost of VDS [3].

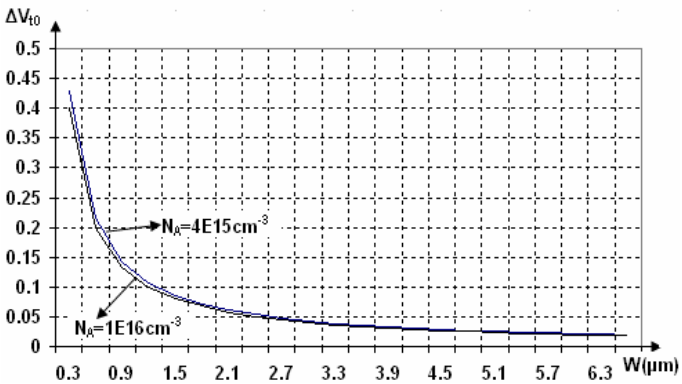

Figure 3. Dependence of ΔVt0 on channel width (W) for parametric values of NA, when ND=1018cm3 and tox=20 nm.

The dependency of the voltage term Vto on the channel width is given in Fig.3, and we can conclude that when W xdm, the Vt term will affect the growth of the total threshold voltage, however when W >> xdm, the Vt term is not important.

A. Threshold voltage calculation of NMOS with short-channel

If the channel length of a MOSFET transistor is on the order of thickness of source and drain junction depletion region, it is referred to as a short channel device. If the effective channel length Leff is almost equal to the S and D junction depth xj, the MOSFET can be classified as a short channel device (Figure 2). The length of the channel has an influence if IGMP is specified as a short channel device. Threshold voltage is a term that refers to the voltage that a device When compared to long channel devices, short channels drop the threshold voltage from V to [4, 5].

$$Vto\ (short\ channel) = Vto\ - \Delta Vto \qquad (1)$$

Let ΔLS and ΔLD denote the lateral extent of the depletion zones associated with the source and drain junctions, respectively, as shown in Fig 3. The charge within the trapezoidal region's bulk depletion region is then:

$$Q_{Bo} = -\left(1 - \frac{\Delta L_S + \Delta L_D}{2\,.\,L}\right)\sqrt{2qN_A\varepsilon_{Si}|-2\Phi_F|} \qquad (2)$$

After calculation the ΔL_S and ΔL_D , the amount of threshold voltage reduction ΔVto can be found as [5, 6]: $-x_{dS}$, x_{dD} represent the depth of depletion regions at source and drain as results of pn junction, respectively.

$$\Delta V_{to} = \frac{1}{C_{ox}}\sqrt{2qN_A\varepsilon_{Si}|-2\Phi_F|}\ \frac{x_j}{2L}\left[\begin{matrix}\left(\sqrt{1+\frac{2x_{ds}}{x_j}}-1\right)\\ +\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)\end{matrix}\right] \qquad (2)$$

B. Threshold voltage calculation of NMOS with narrow-channel

If the channel width of a MOSFET transistor is on the same order of magnitude as the maximum depletion area thickness into the substrate, it is called a narrow-channel device (xdm). When compared to a long-channel device, this effect has an impact on the threshold voltage, resulting in a greater value for Vt0 [7, 8].

$$Vto\ (narrow\text{-}channel) = Vto\ + \Delta Vto \qquad (4)$$

If the geometries of the depletion area edges are described by quarter-circular arcs, the voltage term Vto as a result of narrow-effects is [9]:

$$\Delta V_{to} = \frac{1}{C_{ox}}\sqrt{2qN_A\varepsilon_{Si}|-2\Phi_F|\ \frac{\pi\,.\,x_{dm}}{2\,W}} \qquad (5)$$

After calculating ΔLS and ΔLD, the amount of decrease in threshold voltage ΔVt0 can be calculated as [2, 5]. xdS, xdD signify complexity of the source and drain depletion regions resulting from pn junction. For long channels The device will have a lower threshold voltage if: Substrate doping is reduced (NA), oxide thickness is reduced (tox), oxide interfacial charge is increased (has little effect): Nox) [10]. For short channel devices, the threshold voltage is the Vt term compared to long channel devices, channel length (L), junction depth (xj), drain diffusion doping (small effect), and drain-source. Voltage (VDS).

When compared to long-channel devices, we will enhance the threshold voltage for narrow channel devices by (Vt term), which is dependent on: channel width (W), maximal depletion area thickness (xdm). The positive source-to-substrate voltage VSB causes the rise in total threshold voltage (body effect, as in IC). Finally, for MOSFETs with a restricted channel length and a modest channel width, the threshold voltage variations

caused by short- and narrow-channel effects may tend to cancel each other out [11].

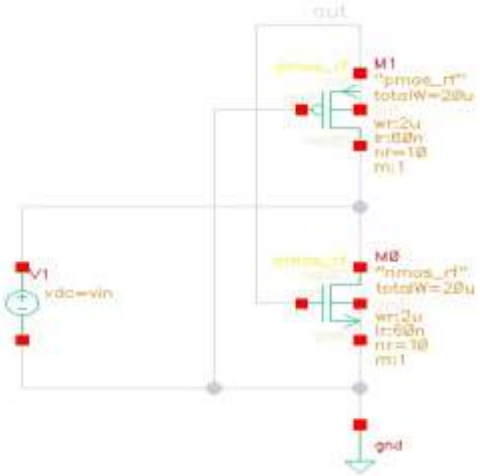

Figure 4. Threshold Voltage cancellation of CMOS Rectifier

Circuit architecture, diode device specifications, RF input signal frequency and amplitude, and output load conditions all impact CMOS rectifier voltage conversion efficiency (VCE) and power conversion efficiency (PCE). The ratio of DC output voltage VOUT to input peak voltage amplitude | VAC | is known as VCE and may be written as :

$$VCE = \frac{Vout}{|VAC|} = \frac{Vout}{Vout+Vdo} \quad (6)$$

Where Vdo is the total dropout voltage along the rectifier's conduction path. PCE is also defined as the ratio of output power Pout to input power Pin. In fact, the PCE of the rectifier is given as follows:

$$PCE = \frac{Pout}{|Pin|} = \frac{Vout}{|VAC|} x \frac{Iout}{Iin} \quad (7)$$

Where Iout is the output DC current and Iin is the total input current of the rectifier.

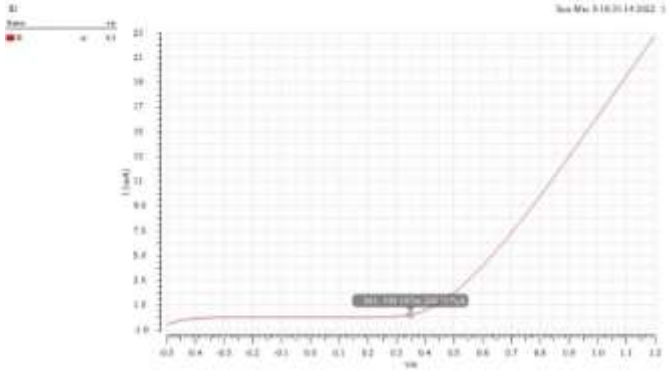

Figure 5.Ooptimize the most effect parameter on Vth cancellation

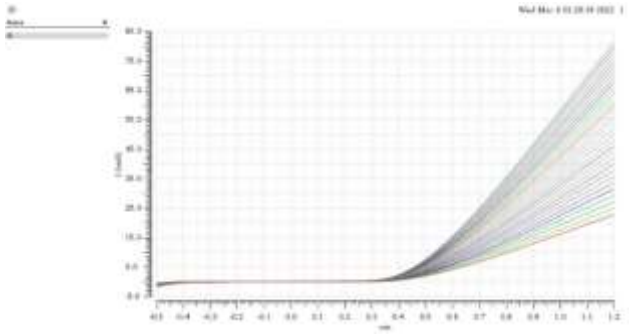

Fig.6. Sweep Analysis of Gate width W with Vth
A slightly change of Vth due to Optimize the Gate width W

II. OPTIMIZATION OF FOUR RECTIFIERS DESIGNS AND SIMULATION RESULTS

As shown in Table.1, the proposed four rectifier circuits were designed using 65nm CMOS technology. We used a cadence tool to perform circuit simulations to optimize performance obtaining the specifications required for proposed design.

The first method cancels MOSFET threshold voltage by applying a gate bias generated from output voltage of rectifier, as shown in Figure 4. This technique provides simple architecture at expense of high reverse current. Upgraded version of the SVC technique is depicted in [8]. 2 Cross-coupled differential CMOS architecture shown in [8] provides better PCE than the SVC scheme. However, the promised VCE will not be provided. An active rectifier architecture based on a 3CMOS inverter is proposed in [9]. It provides good VCE and PCE by reducing both reverse current and threshold voltage. [10,11] uses a technique based on four bootstrap capacitors. Decrease the effective threshold voltage of the main path transistor and increase VCE and PCE.

Table.1 Four Proposed Rectifier Designs

1	Self-VTh Cancellation (SVC) Rectifier	
2	Cross-coupled differential CMOS Rectifier	
3	CMOS Negative Voltage Converter Rectifier	
4	Bootstrapped capacitor-based Rectifier	

The following sections describe in details circuit design parameters and simulation results

A. CMOS Negative Voltage Converter Rectifier

The first stage rectifier design is called the negative voltage converter and is used to positively convert the negative half cycle of input sine wave. This is done using two PMOS transistors and two NMOS transistors, as shown in Figure 7. In the input cycle, node 1 is usually at higher latent and node 2 is at lower latent. As a result, the majority of the MIMO transistors can be connected directly to node 1 and the MIMO can be connected to node 2.

In this case, there is no voltage drop Vth. The voltage drop is only *Vdsp + Vdsn* in each conduction leg. Here, *Vdsp and Vdsn* are generated by the on-resistance of the transistor. Therefore, you can minimize the voltage drop by using a large transistor size to reduce resistance and obtain a small voltage drop.

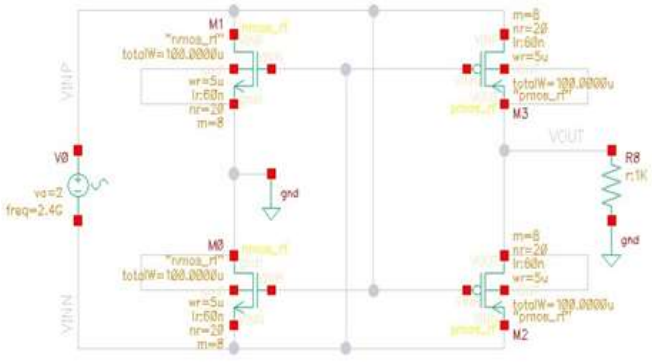

Figure 7a. CMOS Negative Voltage Converter

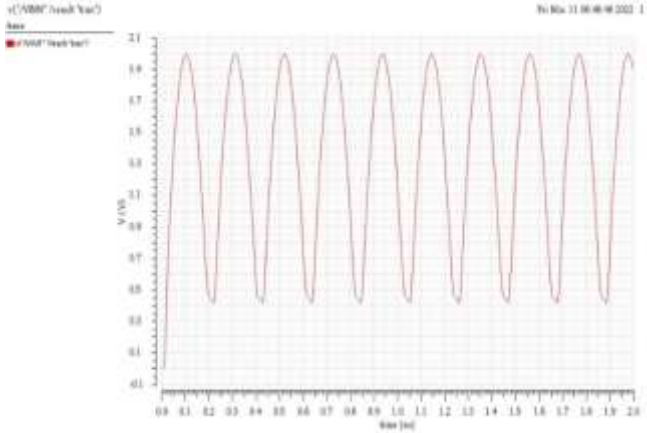

Figure 7b. Waveform of CMOS Negative Voltage Converter. input voltage minimum was 0.35V

B. Self-VTh Cancellation (SVC) Rectifier Design

In recent years, several VTh suppression strategies have been developed to lower the effective threshold voltage in order to obtain high VCE and PCE. [16,17]. The output terminal and ground terminal of the SVC rectifier are linked to the gates of nMOS and pMOS transistors, respectively. It has a straightforward rectifier design with low input power and high PCE. A static gate-source voltage is provided to the MOS transistor in this design, lowering the effective VTh for high DC bias voltage. In recent years, several VTh suppression strategies have been developed to lower the effective threshold voltage in order to obtain high VCE and PCE [12,13]. The output terminal and ground terminal of the SVC rectifier are linked to the gates of nMOS and pMOS transistors, respectively. It has a straightforward rectifier design with low input power and high PCE. A static gate-source voltage is provided to the MOS transistor in this setup, lowering the effective VTh. This architecture increases the reverse leakage current when the DC bias is strong, impacting the VCE and PCE as a whole. The same author presents the improved architecture in [8]. MOSFET threshold voltage is cancelled by applying a gate bias generated from the output voltage of the rectifier. Figure 8a Self-suppressing rectifier (SVC) design. In the SVC waveform in Figure 8b, the input is the blue curve, the red is the output, and the minimum input voltage is excellent, but the maximum is significantly reduced. The minimum input voltage is 0.267V, maximum input voltage being 1.478V.

Because the input signal given by secondary windings of wireless power transfer system is relatively modest, low turn-on voltage is an essential consideration in

diode devices. The relatively high threshold voltage of diode-connected MOS devices limits their performance. Using threshold cancellation methods, VCE and PCE may be greatly boosted. Another aspect that affects the performance of MOS-based diodes is reverse leakage. In order to increase overall performance, different threshold and reverse current suppression strategies for MOS-based diodes have been presented in recent years. In [14,15], the Self Vth Cancellation (SVC) approach is presented.

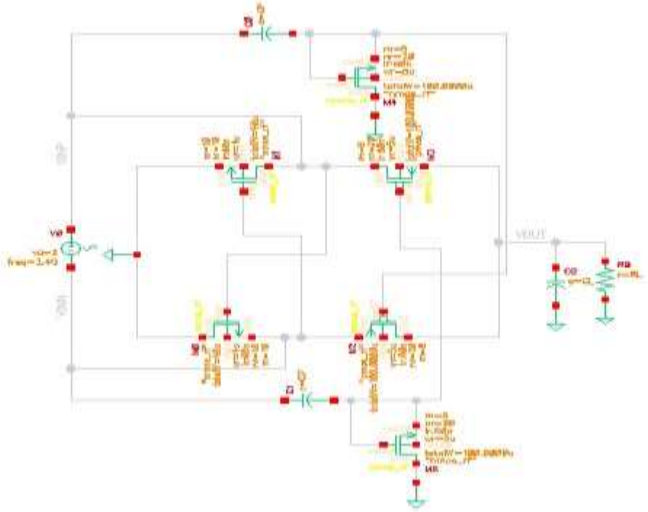

Figure 8a. Self-Vth Cancelation (SVC) Rectifier Design

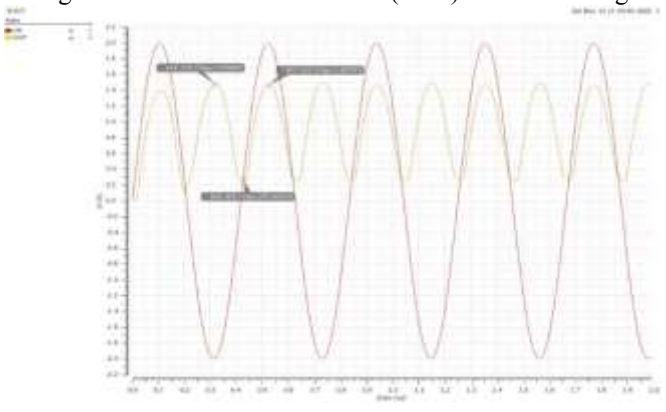

Figure 8b. Waveforms of SVC, The input is the blue curve while red one is the output, the input minimum voltage is better but the maximum is reduced. The min input Volt is 0.267 V while the max input Volt is 1.478 V

C. Differential-drive CMOS Rectifier Architecture

A cross-coupled differential drive CMOS rectifier design is shown in Figure 9. Bridge structure in a cross-coupled differential CMOS system. The differential mode signal actively biases the gate of the MOS transistor in this differential system. With a negative gate bias, this approach efficiently reduces the MOS transistor's on-voltage and rapidly suppresses the reverse leakage current. Although this architecture has a high PCE, it does not have a decent VCE. A decent VCE needs multiple phases, some of which may impose spatial constraints. As a result, this architecture is unsuitable for today's smaller bio-implantable electronics.

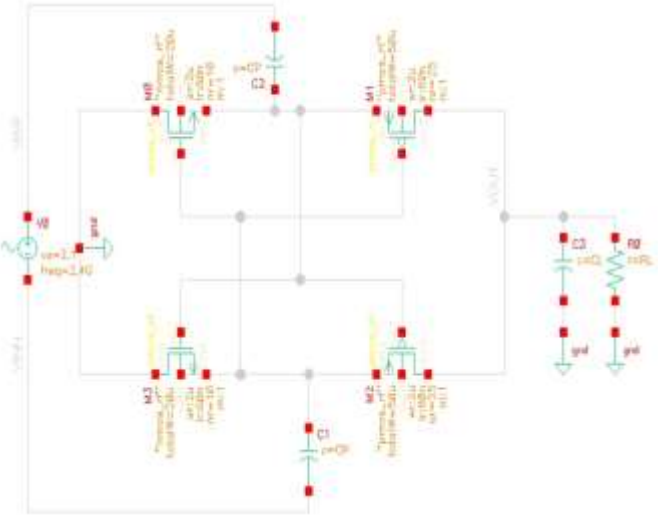

Figure 9a. Design 2 - Differential drive CMOS rectifier

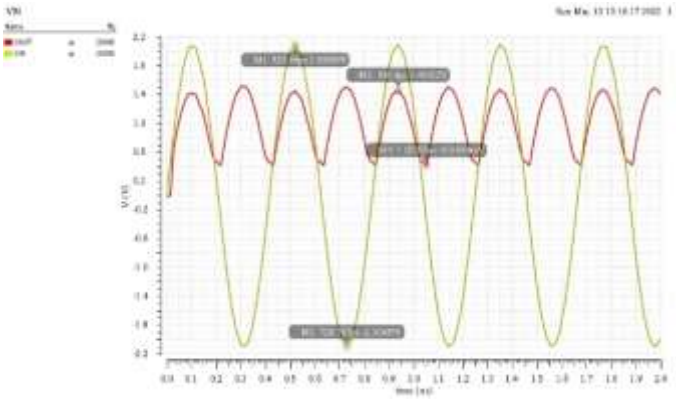

Figure 9b. Waveforms of Differential drive CMOS rectifier

D. Design-3 Bootstrapped capacitor-based rectifier :

To lower the effective threshold voltage, a bootstrap capacitor is employed, and CMOS inverter is used to limit reverse current. High power conversion efficiency (PCE) is achieved at price of low dropout voltage in the planned architecture. The suggested design is well-suited to low-voltage power supply and high-current loads. In a cadence scenario, the suggested rectifier is built in typical 65nm CMOS technology. In comparison to the findings of the best CMOS rectifiers released

recently, the simulation demonstrates that the voltage and power conversion efficiency is enhanced in a limited layout physical -area.

In comparison to [18,19] and 0.28 from 0.5V to 1V, the minimum working voltage is lower, and the rectifier has LIV (low input) with a broad range of input voltage amplitudes from 0.1V to 2.2V. It can operate with voltage). V to 0.7V at [20, 21]. This enables the rectifier to function with a variety of energy collecting systems, including vibration energy harvest, electrostatic energy harvest, electromagnetic energy harvest, and piezoelectric energy harvest.

Voltage efficiency Yv is defined as the proportion of the output DC voltage Vout and the input voltage amplitude |Vin|, as shown in Eq (8). With larger load resistors, the rectifier's output voltage efficiency improves due to its high output voltage drop. [22, 23]

$$\eta_v = Vout / |Vin| = 100\% \quad (8)$$

Power Efficiency of Rectifier is calculated as:

$$\eta_P = \frac{\int_{t_1}^{t_1+T} v_{out}(t) \cdot i_{out}(t)\, dt}{\int_{t_1}^{t_1+T} v_{in}(t) \cdot i_{in}(t)\, dt} \quad 100\% \quad (9)$$

Where T is the duration of the input signal and t1 is the start time. The efficiency drops as RLoad increases because the current through ohmic load decreases and tends to the current through the comparator. The load capacitor, which is tuned for the applied frequency, has a capacitance of 10uF and a load of 50K.

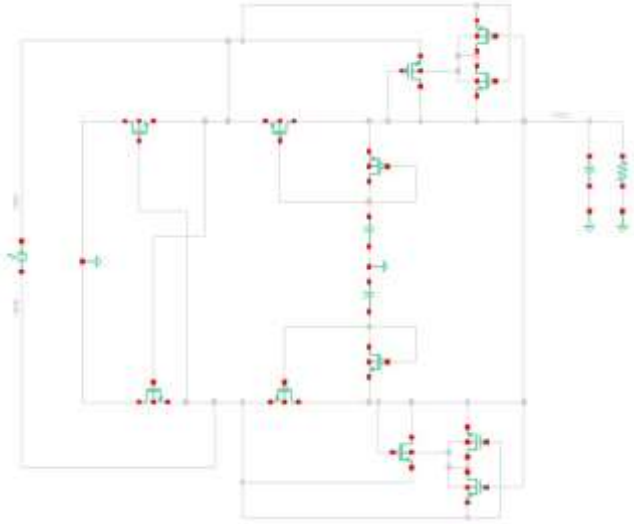

Figure 10a. Design-3 Bootstrapped Capacitor-based Rectifier

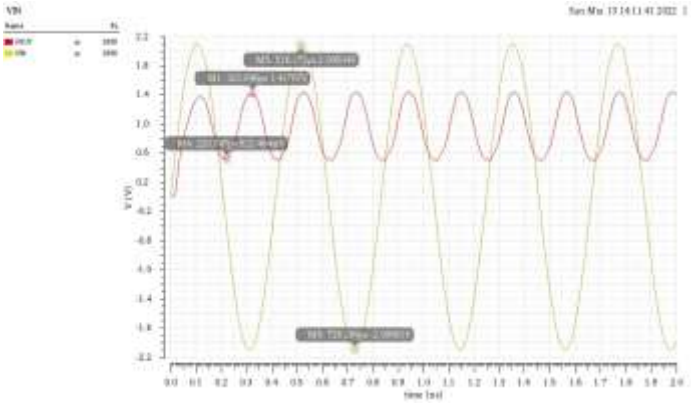

Figure 10b. Waveforms of Bootstrapped capacitor-based rectifier

III. PROPOSED DESIGN OF CMOS RECTIFIERS

This section will involve the schematic, the detailed explanation and layout of two proposed CMOS rectifiers using 65 nm CMOS technology.

A. Differential drive CMOS rectifier with external bootstrapping circuit

1 Description:

The suggested full-wave differential drive rectifier method is depicted in Figure 11. The transistor M2, wired as a nMOS diode, conducts during positive half cycle of the differential input voltage Vin and supplies the current needed to charge the bootstrap capacitor Cp2 (Vina-Vthn).

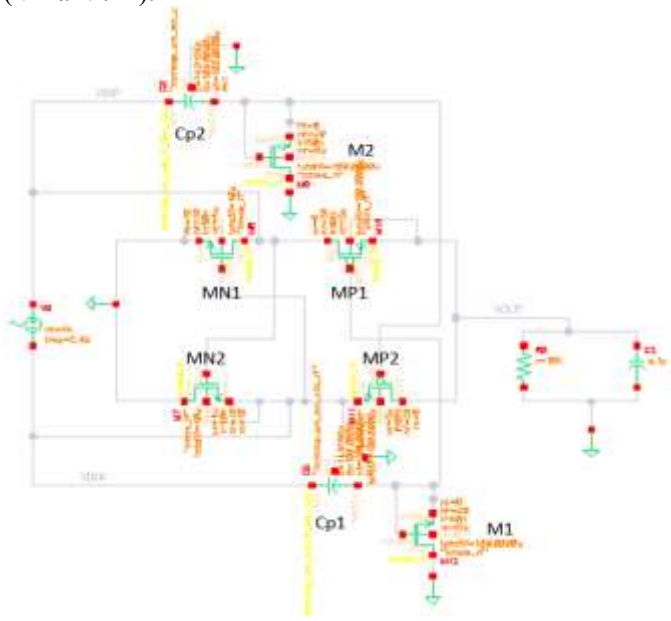

Figure 11. Differential drive CMOS rectifier schematic with external bootstrapping circuit

In the conduction phase, the pMOS switch Mp2 is driven by the sum of the single-ended input voltage Vina and the Cp2 capacitor voltage. The same procedure is used for the pMOS switch Mp1. The gate bias of the pMOS transistors (Mp1, Mp2) becomes more negative than in conventional mode, and the rectifier begins at a lower input voltage. To meet the dynamic threshold compensation method, the body terminals of all transistors are linked to increase their threshold voltages during the off-state and decrease them during the on-state.

Fig.11 shows the schematic of the rectifier working at center frequency of 2.4GHz. The transistor sizes of the NMOS are 400µm but the bootstrapping transistors are 800µm same as the PMOS transistors, bootstrapping capacitors are 15pF. All transistors use the minimum length 60 nm.

Advantages:

- Because the gate bias voltages of pMOS transistors (Mp1, Mp2) become more negative than in the typical mode, the rectifier starts up with a lower input voltage.

Disadvantages:

- Large area due to the usage of capacitors and two diode connected transistors in addition to the 4 transistors used in rectifying the signal.

2 Simulated Results:

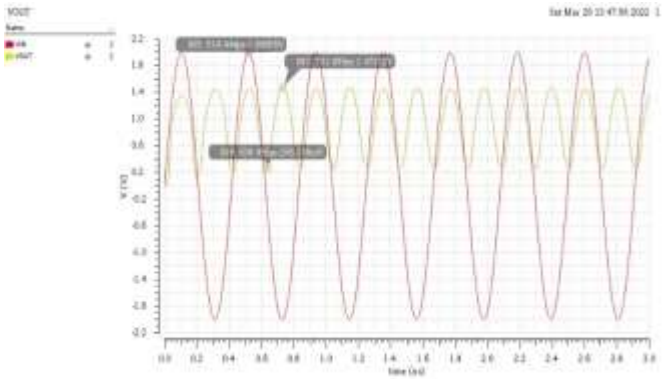

Figure 12. Input and output waveforms at F = 2.4 GHz

3 Performance Summary of Differential drive CMOS Rectifier with external Bootstrapping-circuit at Freq of 2.4 GHz:

With an input voltage amplitude of 2V, the lowest and highest output voltages are 0.265V and 1.467V, correspondingly., peak VCE ($\frac{V_{out}}{V_{in}}$) = 93.9 % and peak PCE ($\frac{P_{out}}{P_{in}}$) = 15.8 %.

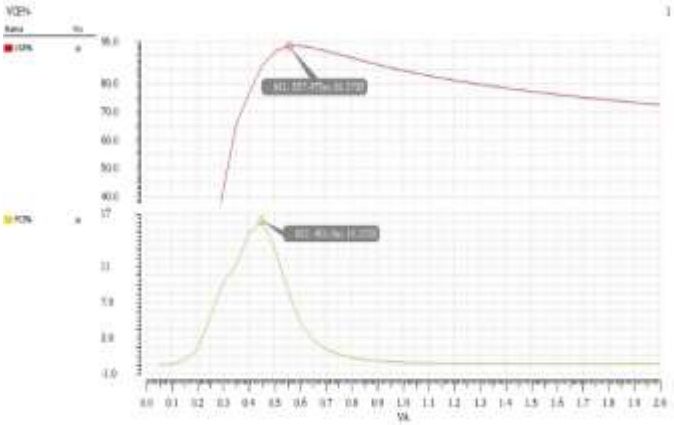

Figure 13. VCE and PCE at F = 2.4 GHz

4 Layout of the Differential drive CMOS rectifier with external bootstrapping circuit:

Figure 14 shows the layout of Differential drive CMOS rectifier with external Bootstrapping circuit. The area of the layout is 0.183 mm x 0.324 mm = 0.059 mm^2. The layout is built using Cadence tools.

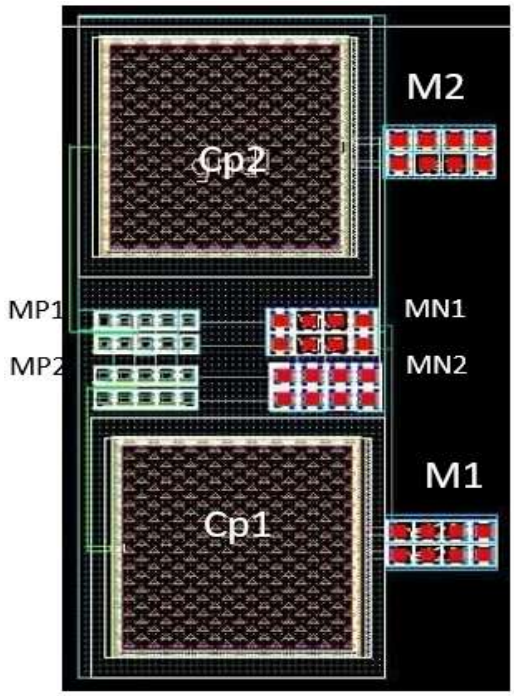

Figure 14. Differential drive CMOS rectifier layout with external Bootstrapping circuit

B. Full-Wave Fully gate cross-coupled Rectifiers (FWFR)

1 Description:
Here transistors act as switches in the positive half cycle M1, M2 transistors are ON and M0, M3 are OFF in the negative half cycle M0, M3 transistors are ON and M1, M2 transistors are OFF. The FWFR proposed design will be given in this section. Fig.15 shows the schematic of the rectifier working at a center frequency of 2.4GHz. The transistor sizes of the NMOS and PMOS are 960 µm and all transistors use the minimum length 60 nm.

Advantages:

- This circuit addresses the issue of diode-tied MOS transistor threshold voltage drop.

Disadvantages:

- The flow-back current from the storage capacitor to the antenna, as well as other parasitic currents, reduce the power efficiency of this device.

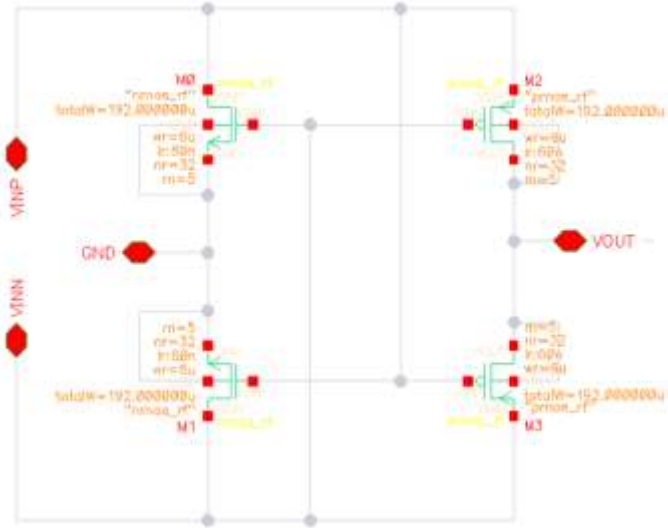

Figure 15. Schematic View of FWFR CMOS Rectifier

2 Simulated Results:

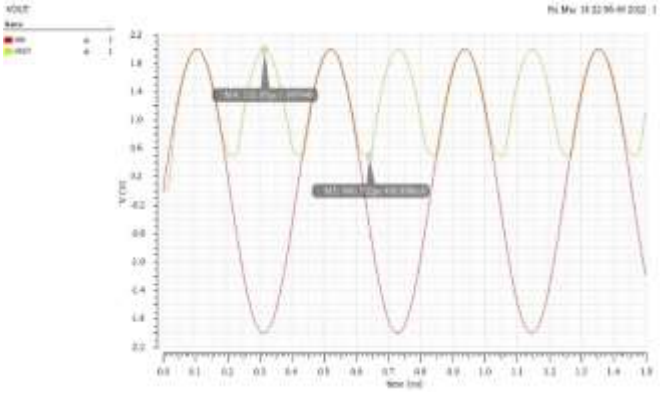

Figure 16. Input and output waveforms at F = 2.4 GHz

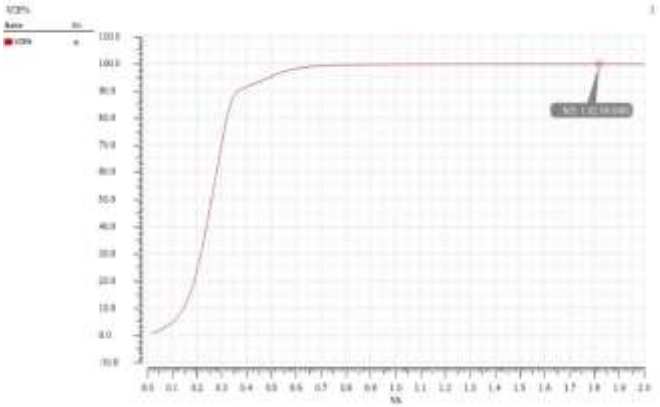

Figure 17. VCE at F = 2.4 GHz

3 Performance Summary of FWFR CMOS Rectifier at Freq of 2.4 GHz:
The minimum and maximum output voltages generated using input voltage amplitude of 2V are 0.49V and 1.997V respectively, maximum VCE ($\frac{V_{out}}{V_{in}}$) = 99.85 % and maximum PCE ($\frac{P_{out}}{P_{in}}$) = 46.86 %.

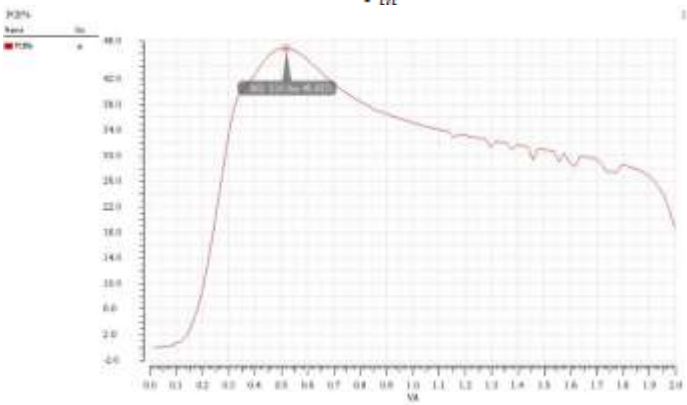

Figure 18. PCE at F = 2.4 GHz

4 Layout of the FWFR CMOS Rectifier:

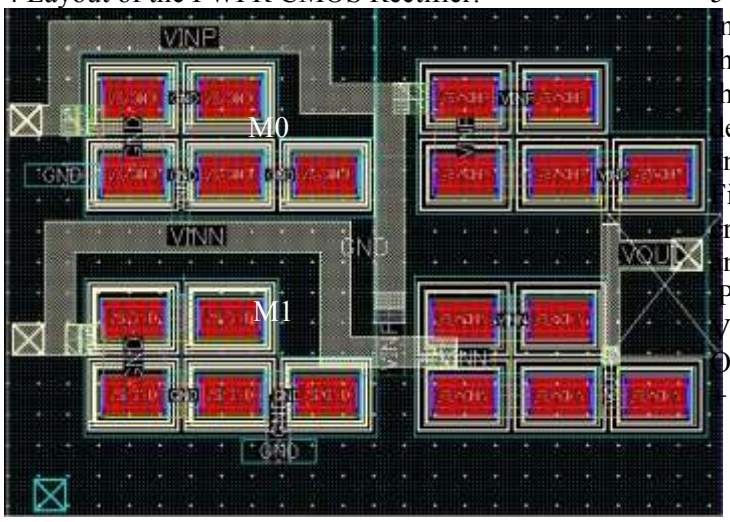

Figure 19. Layout of the FWFR CMOS Rectifier

Fig.19 shows the layout of second proposed CMOS Rectifier, taking into consideration the widths of the wires. The area of layout is 0.117mm x 0.079mm = 0.009mm2. The layout is built using Cadence.

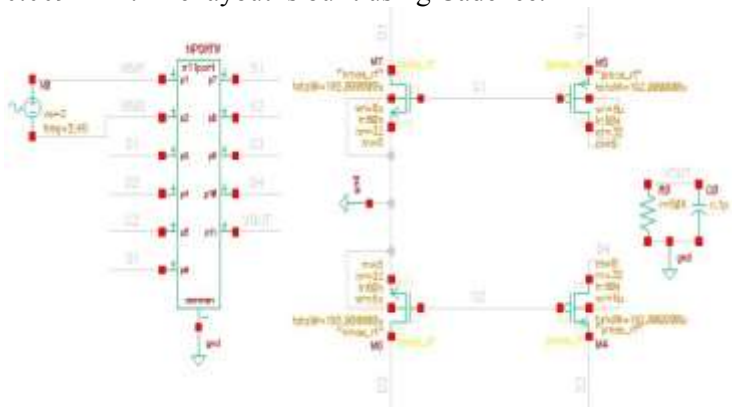

Figure 20. EM simulations for wires connection

Figure.20 show the EM simulations for all the wires connecting between the 4 transistors and made the required sp file

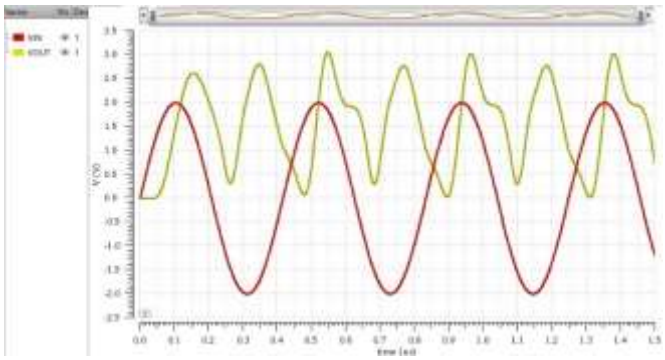

Figure 21. The red curve is the differential input and the yellow one is the output one

5 Performance comparisons:

n this section we compare our proposed designs among hemself and compare the best two designs compared to he previous research. In order to be able to rank the esigns, we identified the most important factors PCE nd VCE and follow ranking methodology described in ig.20. According to flow chart in Fig.20, the selection riteria was done by giving score for both PCE and VCE nd calculate weighted average score as follows:

PCE Score (%) = PCE %/ PCE % best score (a)

VCE Score (%) = VCE % / VCE % best score (b)

Overall Score Average Score = 50% * PCE Score (%) + 50% * VCE (Score%) (c)

Figure 22.. Ranking methodology of Rectifier Designs

Table.2. provide detailed of all results and Design Performance assessment based on our proposed assessment methodology in Fig.20. According to Table.2. we selected the top two options and perform detailed layout using Cadence Layout module. The model show that first rank is cross coupled FWFR CMOS rectifier topology and second is differential drive rectifier topology . As final conclusion we found the first rank has net area XX mm2 and second rank has xx mm2 so by selecting the minimum layout area the best option will be YY model.

Table 2. All Results of Proposed Designs and Assessment

Parameters	**First Design**	**Second design**	**Third Design**	**Fourth Design**
Rectifier Topology	Cross Coupled	Differential Drive	Bootstrapped Capacitor	Vth-Cancellation
Vout DC	419.68mV - 1.464 V	522.46 mV - 1.4176 V	265.515 mV - 1.467 V	490.868 mV - 1.997 V
PCE %	30.55%	13.85%	15.787%	46.855%
VCR % S	94.4%	64.19%	93.91%	99.849%
Score Output Range	69.3%	59.4%	79.8%	100%
Score PCE%	65.2%	29.6%	33.7%	100%
Score VCE%	94.5%	64.3%	94.1%	100%
Score Average	76.3%	51.1%	69.2%	100%
Score Overall	**Second**	**Fourth**	**Third**	**First**

Table 3. Performance Parameters Comparisons between Low Voltage Rectifiers

Performance Parameters	IEICE 2012 [15]	IEEE TCAS I 2011 [16]	**Differential drive Rectifier**	**Cross Couple FWFR CMOS**
Technology	0.18um CMOS	0.18um CMOS	65nm CMOS	65nm CMOS
Input Voltage Amplitude	0.28V-0.7V	0.5V-1V	0.21V – 1.95V	0.2V – 1.45V
Working Frequency	10Hz-3KHz	10Hz-10KHz	2.4GHz	2.4GHz
|Vmin|	0.28V	0.5V	0.21V	0.2V
Voltage Efficiency	76%-97% (R_{Load}=40 k)	90% (R_{Load}=50k)	94.5 %	71%-81% (R_{Load}=50 k)
Power Efficiency	78%-95%	Up to 95%	94.5%	73% -79%

Table.3 compares the performance of this study to that of other rectifiers previously published. Previous rectifiers' lowest functioning voltage was 0.5V in [17] with a 0.5V low threshold voltage 0.35um CMOS technology. When the input voltage is more than 1V, however, it will not operate, and the application field will be blocked. These flows are addressed by the rectifier suggested in this work. It can not only work with a 0.45V input voltage, but also with input voltage amplitudes ranging from 0.45V to 1.95V, as opposed to 0.5V to 1V in [24] and 0.28V to 0.7V in [25, 26].

In this study, an energy harvesting system with a wide range input voltage amplitude and a highly efficient rectifier is suggested. Under the 65nm CMOS process, the rectifier is ideally suited for input amplitude as low as 0.2V and can function at a wide range of input voltage amplitudes from 0.2V to 2.1V. The suggested rectifier has a maximum voltage conversion efficiency of more than 81% percent and a power efficiency of more than 79% percent. The rectifier's simulated power usage is 0.23 uW at 0.45V, which is approximately 28% less than that of the finest recently reported findings.

IV. CONCLUSIONS

The proposed rectifiers are designed for 2.4GHz using a two-stage assembly and an enhanced accuracy active diode in a standard 65nm CMOS process. The lower most operating voltage is less than in the earlier studies, and the rectifier can operate with input voltage amplitudes ranging from 0.2V to 1.95V. This enables the suggested rectifier to be used in a variety of vibration energy collecting systems, including electrostatic, electromagnetic, and piezoelectric energy harvesters. The suggested rectifiers have a highest voltage conversion efficiency of over 81% and a power efficiency of over 79%. The rectifier's simulated power consumption at 0.45V is 0.23 uW, which is roughly 28% less than the best recently reported findings. Mechanical vibrations are the most common energy source accessible in many contexts, which is a benefit of employing them to capture energy.

The proposed rectifier, which is built at 2.4GHz and has a two-stage structure, performs better in the event of low input voltage amplitude and has a lower minimum operation voltage than previously published papers. Full-wave fully gate cross-coupled rectifiers (FWFR) CMOS Rectifier Performance Summary at Freq of 2.4 GHz: With a 2V input voltage amplitude, the minimum and maximum output voltages are 0.49V and 1.997V, respectively, with a maximum VCE of 99.85 percent and a maximum PCE of 46.86 percent. At Freq of 2.4GHz, the performance of a differential drive CMOS rectifier with an external bootstrapping circuit rectifier is summarised as follows: With a 2V input voltage amplitude, the minimum and highest output voltages are 0.265V and 1.467 V, respectively, with a maximum VCE of 93.9 percent and a maximum PCE of 15.8 percent.

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