oscillator output is divided into odd and even groups, leaving enough processing time for compensation.

The 0.5Hz square signal uses as a control, the odd-numbered second (2n+1) counter enables at a high level, and the even-numbered second (2n+2) counter enables at a low level. Determine how to compensate the clock source according to the counter and the theoretical value difference. If the difference is negative, pulse needs to add, and if the difference is positive, pulse needs to delete.

The fundamental clock frequency is 4.096MHz, and the accuracy is 70ppm, so the maximum number of errors counted in one second is 280. The pulse compensation should be equally divided within 1s. This article divides the 4.096MHz oscillation into 512 groups. The number of compensation pulses *n* should be distributed in the first *n* groups of 512.

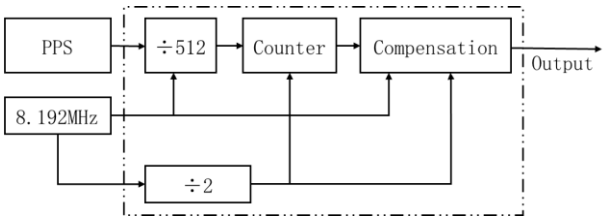

Fig. 6 block diagram of clock source for group compensation

The Block diagram of the clock source for group compensation is as shown in Figure 6. The 8.192MHz crystal oscillator is divided by 2 to obtain 4.096MHz as the fundamental clock. The output of the crystal oscillator is frequency-divided to generate a 512Hz signal. If the compensation difference is negative, replace the current pulse with an 8.192MHz pulse. Figure 7 shows the compensation for this situation. If it is positive, set the output low. Figure 8 shows the compensation for this situation.

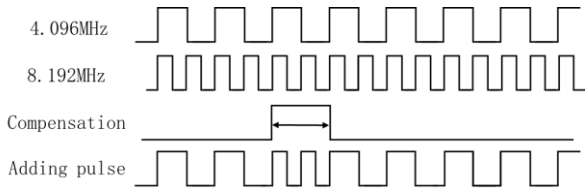

Fig. 7 the principle of compensation for adding pulses

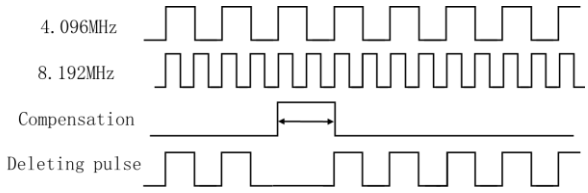

Fig. 8 the principle of compensation for deleting pulses

When starting to count, there is uncertainty in the clock phase at the starting time. Therefore, it is necessary to include a fundamental clock of 8.192MHz with a clock period of 125ns while calculating the error.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

The time synchronization system in consists of a surface module and borehole module. The surface module sends the PPS to the monitoring node in the borehole. It is composed of a GPS board and an FPGA board. Figure 9(a) shows the GPS board. Figure 9(b) shows the FPGA board. The GPS board communicates with the computer through the network and controls the FPGA board to send PPS. The FPGA board in the monitoring node is responsible for delay compensation and clock reference source, as shown in Figure 9(c).


(a) GPS board


(b) FPGA board


(c) the monitoring node`s FPGA board

Fig. 9 the composition of the time synchronization system

To verify the accuracy of the synchronization system, the above modules were tested separately. The length of the logging cable used for the test is 3000 meters. The measuring equipment is a Tektronix MDO4054C oscilloscope with a bandwidth of 500MHz and a sampling rate of 2.5GS/s. In the test, use it to capture and display the waveform.

A. *Delay measurement test*

This section tests the delay caused by the transmission of PPS. Channel 1 of the oscilloscope measures the pulse signal output from the logging cable, and Channel 2 measures the pulse signal input to the logging cable.

Figure 10 shows the PPS send at the surface module with a 10% duty cycle. Figure 11 is the PPS measured at the surface module and borehole module. Figure 12 compares the rising edges of the two waveforms from Figure 11. It can find that the transmission of the PPS through a 3000*m* cable produces a delay of about 18.6 *us*.

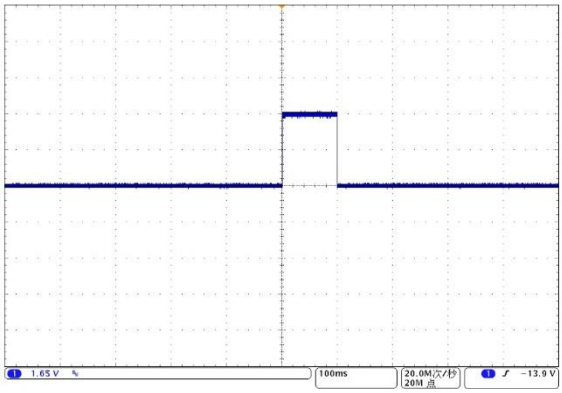

Fig. 10 a simulated PPS

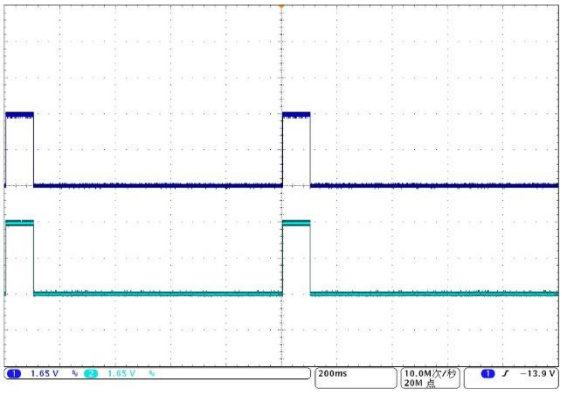

Fig. 11 PPS at the transmitter and receiver

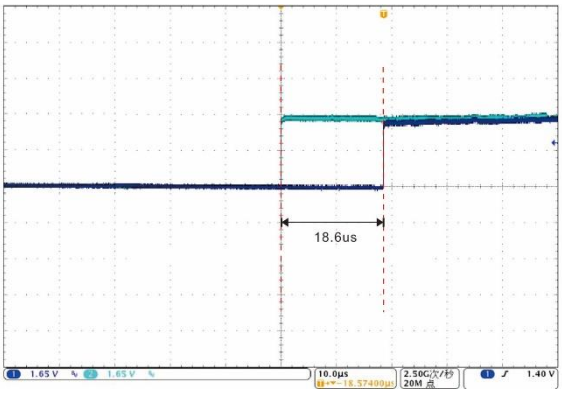

Fig. 12 delay caused by PPS transmission via cable

B. *Delay compensation test*

This section compares the difference between the compensated pulse and the PPS generated by the GPS. Channel 1 of the oscilloscope measures the compensated pulse, and channel 2 measures the PPS, the comparison results shown in Figure13. It can find from the rising edge comparison in Figure 14, and the difference is 38.4*ns*.

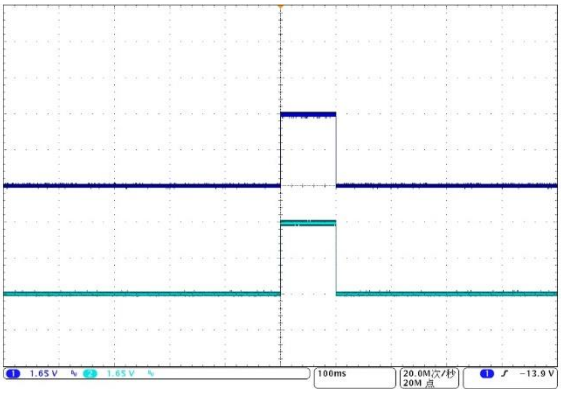

Fig. 13 waveform comparison of PPS

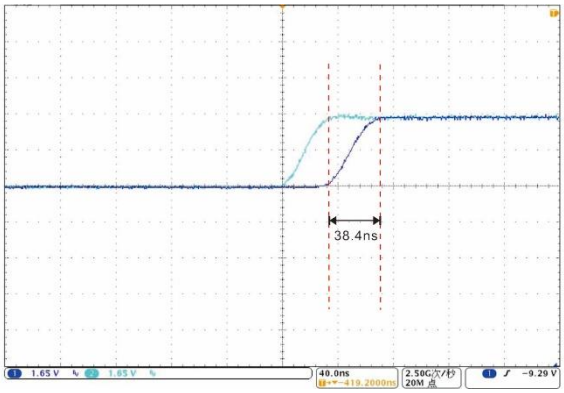

Fig. 14 waveform comparison of PPS rising edge

Five tests were carried out to verify the stability of the delay compensation module. The interval between each test ranged from 1 to 2 days. Ten measurements were taken for each test. The measurement results show in Table 1. The table's average value of the measurement data is 50.7*ns*, and the mean square error is 8.6*ns*.

Table 1 the measurement results (ns)

No.	Test1	Test 2	Test 3	Test 4	Test 5
1	38.4	53.3	64.1	36.6	59.3
2	36.1	56.0	55.3	64.9	50.2
3	61.3	45.5	62.9	62.2	46.3
4	56.4	48.8	48.9	51.3	48.2
5	45.6	60.1	60.9	51.1	47.9
6	55.8	60.5	64.7	48.6	48.8
7	36.6	48.2	44.5	62.1	64.4
8	43.5	49.1	36.9	60.5	58.9
9	53.0	52.1	48.4	52.5	52.6
10	39.1	53.3	36.3	37.0	40.9

C. *Clock reference source test*

This section measures the compensation of the clock source. The Chipscope logic analyzer component of the ISE software uses to measure the compensated clock. The output of the crystal oscillator triples by FPGA and operates as the sampling clock of the logic analyzer to measure the clock source. Figure 15 is the waveform of the adding pulse, and Figure 16 is the waveform of the deleting pulse.

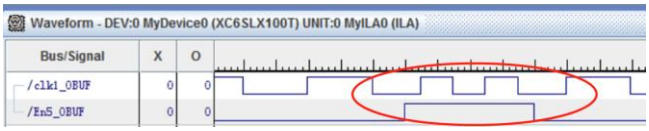

Fig. 15 the waveform of the adding pulse

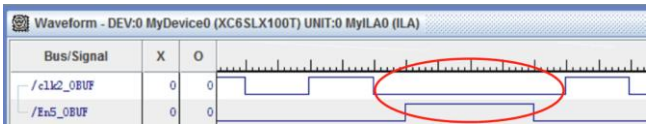

Figure 16 the waveform of the deleting pulse

We compare the monitoring data from the borehole and surface to verify the validity of the clock source under long-term operation. The borehole and surface nodes are placed in the same environment and generate seismic waves by hitting the ground.

The first step is to use an uncompensated clock source for data acquisition. After a few hours of regular work, we conducted a data test. Figure 17 shows the waveforms acquired from the same hitting event by borehole and surface nodes. Figure 18 selects 200 consecutive sampling points for comparison. The number of sampling points has begun to deviate through contrast, about 4 to 5 sampling points.

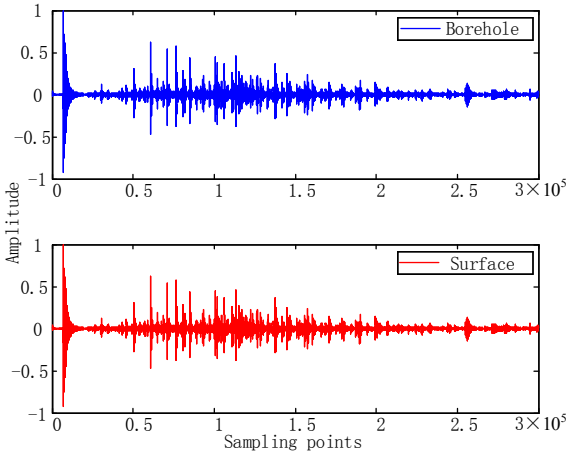

Figure 17 comparison of monitoring data with an uncompensated clock source

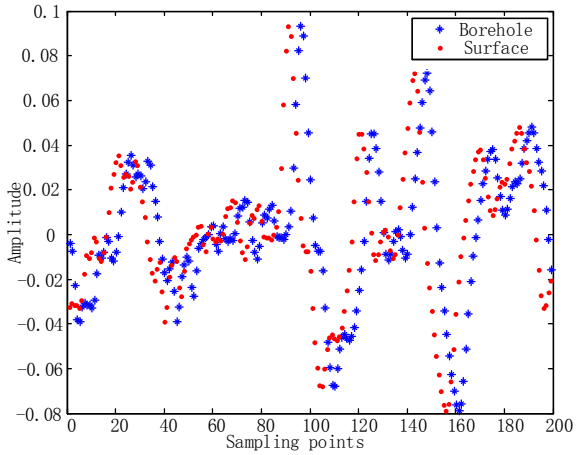

Figure 18 select 200 points to compare an uncompensated clock source

The second step is to use a compensated clock source for data acquisition. Similarly, after a few hours of regular work, we conducted a data test. Figure 19 shows the waveforms acquired from the same hitting event by borehole and surface nodes. Figure 20 selects 200 consecutive sampling points for comparison. Through comparison, it can find that the sampling points are very close, and the sampling time interval between the two sampling points is close to 400ns.

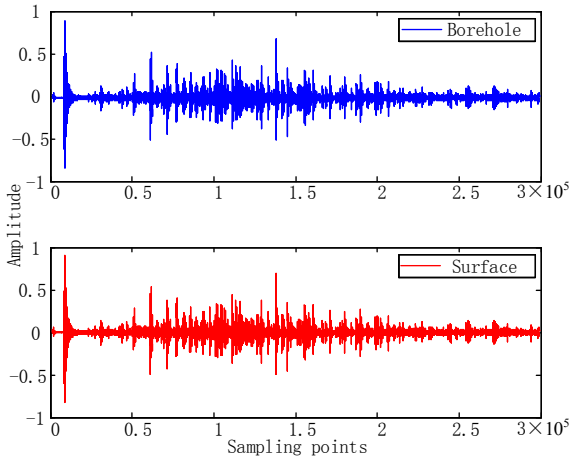

Figure 19 comparison of monitoring data an compensated clock source

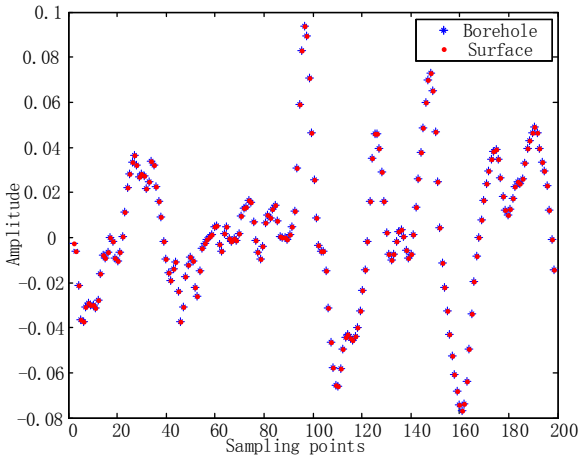

Figure 20 select 200 points to compare an compensated clock source

V. Conclusion

This paper focuses on the synchronization signal delay caused by the cable transmission. The temperature-compensated crystal oscillator is used on the surface to measure the delay, and the high-temperature crystal oscillator is used in the borehole to compensate. Aiming at the high-temperature crystal oscillator's accumulated error in the borehole, compensation methods propose the delay compensation module and the ADC clock source, respectively. The method in this paper can ensure that the error between the initial sampling point of the ADC in the borehole and surface is less than 100ns. To compensation the ADC clock source, we use PPS to count the crystal pulses at a fixed time interval and decide whether to insert or delete pulses. The pulse compensation divides into multiple periods of 1s. This method can control the synchronization error of the ADC within 400*ns*. The experiment results show that the proposed method can strictly synchronize the monitoring data in the borehole with the monitoring data on the surface. We will build a deep learning model on the crystal oscillator's offset compensation to suppress the accumulated error in future work.

Acknowledgment

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy) Yadongyang Zhu proposed a calibration method to compensate for the deviation of time synchronization due to long-distance transmission on the logging cable. Yadongyang Zhu and Wenhao Wei conducted the experiments and analyzed the results. All authors discussed the results and wrote the manuscript.