Massive Speech Recognition Resource Scheduling System based on Grid Computing

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Abstract—Nowadays, there are too many large-scale speech recognition resources, which makes it difficult to ensure the scheduling speed and accuracy. In order to improve the effect of large-scale speech recognition resource scheduling, a large-scale speech recognition resource scheduling system based on grid computing is designed in this paper. In the hardware part, microprocessor, Ethernet control chip, controller and acquisition card are designed. In the software part of the system, it mainly carries out the retrieval and exchange of information resources, so as to realize the information scheduling of the same type of large-scale speech recognition resources. The experimental results show that the information scheduling time of the designed system is short, up to 2.4min, and the scheduling accuracy is high, up to 90%, in order to provide some help to effectively improve the speed and accuracy of information scheduling.

Keywords—Grid Computing; Massive; Speech Recognition Resources; Same Type; Information Scheduling.

I. INTRODUCTION

The task of resource scheduling system is to manage and schedule all resources in the system, reasonably arrange the use of resources, and effectively provide real-time services for all kinds of users. And it is the control center of the whole voice information management system, which can receive and process the request response of each workstation. Because there are a lot of speech resources, it is difficult to schedule speech recognition resources effectively. Therefore, it is urgent to study the resource scheduling method [1].

At present, some scholars have carried out research on this. Du et al. studied a two-dimensional resource adaptive scheduling algorithm [2]. Based on the recognition of target characteristics, according to the principle of compressed sensing, calculate the pulse resources required for two-dimensional sparse observation of targets, and then design a two-dimensional resource scheduling model to realize the adaptive allocation and scheduling of two-dimensional pulse resources [2]; Zhao Gang studied a network data resource scheduling system [3]. Firstly, the overall scheduling structure of the system is designed, then the ship network data resource feature management module is designed, and finally the ship network data resource scheduling module is designed to complete the data resource schedulingt [3]; Sun et al. studied a spectrum efficient and fair resource scheduling method [4]. Firstly, the transmission data rate of MBMS group is selected according to the link adaptation and the average packet loss rate of users, and then the system throughput and user fairness are further balanced to realize data resource schedulingt [4].

Although the above scholars have carried out research on

this, the above methods are difficult to effectively improve the speed and accuracy of information scheduling. Grid computing is a kind of distributed computing and a computer science. It studies how to decompose a problem with large amount of calculation into many small parts, then assign these small parts to multiple computers for processing, and finally synthesize these calculation results to get the final result. Moreover, it can meet the needs of users distributed in different regions and realize resource sharing and collaborative work. In order to improve the effect of information scheduling, grid computing is introduced into this field. In the hardware part, microprocessor, Ethernet control chip, controller and acquisition card are designed. In the software part of the system, it mainly carries out the retrieval and exchange of information resources, so as to realize the information scheduling of the same type of large-scale speech recognition resources, in order to provide some help to effectively improve the speed and accuracy of information scheduling.

II. HARDWARE DESIGN OF THE SAME TYPE INFORMATION SCHEDULING SYSTEM FOR MASSIVE SPEECH RECOGNITION RESOURCES

A. Microprocessor design

S3C2440A is Samsung's embedded microprocessor chip based on ARM⑨20T core. The processor supports 16 bit and 32-bit reduced instruction set (RISC), adopts 0.13um CMOS standard memory and macro unit, and integrates some commonly used peripheral components. Its limiting dominant frequency can reach 53MHz, but the maximum stable operating frequency is about 400MH. It is a low-power, high-performance microprocessor ARM920T is a kind of embedded processor which is widely used in handheld devices at presen. It is a prominent feature of S3C2440A. ARM920T has 16KB instruction Cache, 16KB data cache and MMU. It is a high-speed data buffer architecture which supports AMBA bus interface and five level pipeline Harvard structure. S3C2440A has a complete set of system on chip peripherals. The advantage of S3C2440A is that it saves the design of peripheral components, saves the development time and economic cost, and improves the stability of the system. According to the function description of the chip, the main functions of

S3C244A are as follows:

(1) Supporting power supply to 12V kernel, power supply for three kinds of storage devices of 3, 3V, 2.5V and 1.8V, and power supply to external input and output pins of 3.3 V. It has 16KB instruction Cache and 16KB data Cache and memory management unit;

(2) Supporting the control of external SDRAM;

(3) It has 3 independent UART serial ports;

(4) It has 1 8-channel 10 bit AD converter;

(5) It has two USBHOST interfaces and one DE VICE interface;

(6) Supporting the control of STN LCD with 4K color and 256K TFT LCD, and control the LCD screen;

One channel DMA is provided;

(7) Real Time Clock RTC;

(8) It has 4 channel DMA for external IO requests;

(9) It has 130 universal IO pins and 24 external interrupt sources, and 4 timers supporting PWM output.

B. Design of Ethernet control chip

DM9000 is a cost-effective Fast Ethernet control chip developed by Taiwan's Lianjie international company. The main function of the chip is to complete the data interaction between the physical layer and the data link layer of network communication. The chip has a 10 / 100M bandwidth adaptive physical layer interface, which meets the requirements of IEEE8023u. With the support of its physical layer interface protocol, dm9000 completes the maximum bandwidth adaptation, supports the tolerance of 33V-5V, has a 4K double byte data memory [5-7], and supports full duplex flow control. DM9000 network card is exquisitely designed, and supports the operation of 8-bit, 16 bit and 32-bit hardware interfaces on its internal memory. Therefore, DM9000 supports the application of multiple processors. S3C2440A embedded microprocessor uses 16 bit interface to connect with dm9000, 1or of dm9000 network card interface chip is the read control pin, which is connected with the NOE pin of S3C2440A; IOW # pin is the write control pin, which is connected with NWE pin of S3C2440A; int pin is the terminal output pin, which is connected with eint18 of S3C2440A, which makes S3C2440A respond to the interrupt of DM9000; SD [.15] pin is DM The data interface of DM9000 is 16 bits wide, which is connected with IO data [o.15] of S3C2440A to complete the data transmission between them; the status of the CMD pin of dm9000 is used to distinguish whether the

data information or command information is transmitted between them; when the CMD level is low, it means that the address port is selected; When the CMD level is high, it means that the data port is selected, which is the same as that of S3C2440A The chip select pin NGCS4 of DM9000 is connected to the chip select signal input pin of DM9000, and the address line pin ADDR2 of S3C2440A is connected to the chip select signal input pin of DM9000.

C. Design of controller

The controller used in this design is STM32F103ZET6, which is an ARM microcontroller with 32-bit Cortex-M3 core, and its maximum working frequency can reach 72MHz. The core circuit includes microcontroller, crystal oscillator circuit, reset circuit, memory and power supply circuit. Among them, the microcontroller adopts STM32 Ⅳ 103ZEr6 chip with 14 pins. The crystal oscillator circuit generates clock signal for the controller and provides clock pulse [8-11] during the operation of the controller. The reset circuit adopts hardware reset mode, and the reset operation makes the system recover from the working state to the initial state when the system is powered on; the power supply voltage stabilizing circuit is the core component of the power supply. The power supply of the power supply module in the minimum system can be supplied by the external stable 5V power supply module.

D. Design of data acquisition card

Two problems must be considered in a multi-channel digital audio system: the quality of the collected sound and the storage of the final digitized audio. According to Nyquist's theorem, if we want to recover the collected audio signal completely, the sampling rate must be less than twice the bandwidth of the collected audio signal.

The multi-channel audio acquisition card based on FPGA and DSP is adopted, and the cyclone series FPGA of Atea company is used to simplify logic control and improve hardware speed; the TMS320VC5416 of ∏ company is used to realize audio compression algorithm, which not only meets the audio performance index, but also reduces the final audio data and meets the design requirements of the system. The structure of the acquisition card is as follows:

Firstly, the main chip selection, in the audio CODEC chip selection, using the PCM3008 of Texas Instruments. This codec chip adopts 16bit 4-∑ADC Sigma ADC and DAC. The stereo ADC has a single terminal voltage input

and built-in anti aliasing filter. The excellent performance is not shown in the fact that the total distortion and noise of the ADC is as low as -84 dB. The built-in 1 / 64 Decimation digital filter makes the signal fluctuate only 005dB in the passband and the stopband attenuation can be as low as -65 dB. Low voltage operation, low power consumption [12-15]. The sampling rate is 8 kHz-48 kHz. Data transmission is synchronous serial port mode, easy to operate.

Secondly, the FPGA chip EP1C6Q240FPGA uses the EP1C6Q240 of Cyclone series of Atea company to realize the interface control of each device. FPGA of Cyclone series is launched by Atea company for low-cost and high-performance applications, with high cost performance. EP1C6Q240 has 185 maximum available O, 92 Kb RAM can be used as single and dual port RAM, ROM, HFO and other memory modules, and two high-precision phase-locked loops can conveniently provide the required clock for each module in the chip: 5980 LE (logic unit), which provides rich logic resources for the implementation of interface circuit, and the logic analyzer provides great convenience for the user's debugging.

Thirdly, DSP chip adopts TMS320VC5416 of ∏ company. TMS320VC5416 is a fixed-point DSP with high performance and low power consumption in T company 5000 series, which is based on C54XDSP core. TMS320℃5416 is a 16 bit fixed-point high-performance digital signal processor. Its main features are: up to 160MPs speed; three 16 bit data memory buses and one program memory bus; one 40 bit barrel shifter and two 40 bit accumulators; one 1717 multiplier and one 40 bit special adder; maximum 8M16 bit extended addressing space; built-in 128k16 bit ram and 16k16 bit ROM; three multi-channel buffers. With its rich peripherals and powerful computing power, TMS320VC5416 can carry out real-time multi-channel audio processing. In the implementation of compression, the use of general DSP chip TMS320VC5416, compared with the use of dedicated hardware compression chip, can not only save the cost, but also easily achieve the system upgrade and flexible configuration, the structure is shown in Fig. 1:
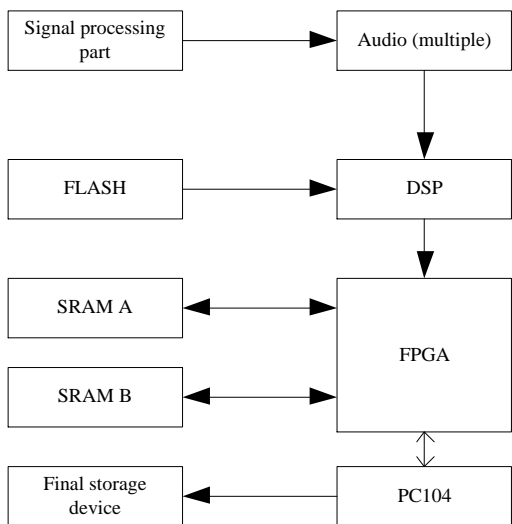
Fig. 1 DSP chip structure

Fourth, the FPGA function module design, FPGA design uses the modular design idea. The SRAM controller adopts ping-pong mechanism, one is in the state of reading data, the other is in the state of writing data, and switches once every 15 seconds under the control of PC104 host. The timing design of this operation mode is simple and reliable, and it is easy to achieve continuous audio data acquisition. After receiving the switch command from the PC104 host, when both SRAMs are idle, the read-write switch of the two SRAMs is completed. At the same time of switching, the read and write addresses of SRAM will be reset, and the data volume information in the previous 15 seconds will be saved, so as to ensure that each 15 second read and write starts from the zero address, which is also convenient for reading data. After the switch is successful, the data ready signal is displayed, indicating that the host can read the data. PC104 interface module is responsible for the communication and data transmission between the acquisition card and the host computer. Complete the read and write switching of two SRAMS. At the same time of switching, the read and write address of SRAM will be reset, and the data amount information in the previous 15 seconds will be saved, so as to ensure that the read and write of every 15 seconds start from the zero address, and it is also convenient to read data. After the switch is successful, it indicates that the host can read the number. The functional modules of FPGA are shown in Fig. 2 below:
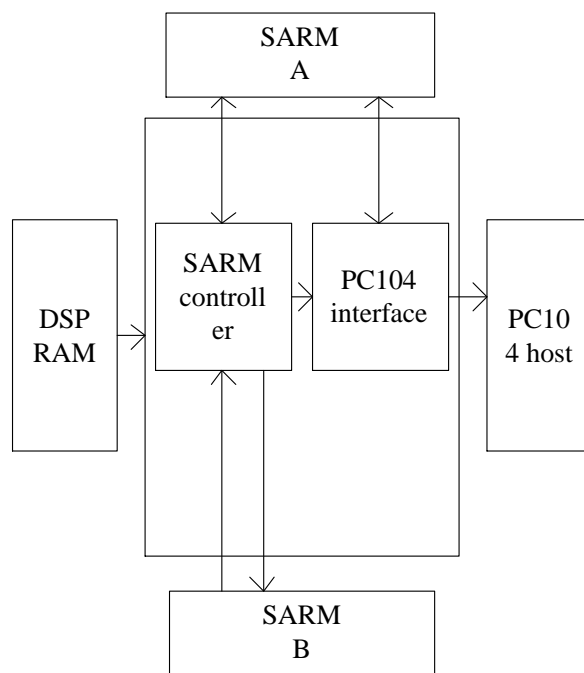
Fig. 2 Function module of FPGA

DSP uses MBSP to communicate with audio CODEC. MCBSP relies on three signals to receive data: data line DR, frame synchronization line FSR and shift clock line CLKR. The DR pin receives the audio data from the audio codec, and the CLKR.FSR realizes the control of clock and frame synchronization. When receiving data, the data from the DR pin is read out from the data register DRR under the action of FSR and CLKR. CLKR and FSR can be generated by internal sample rate generator or driven by external devices. In this audio system, CLKR and FSR signals come from FPGA. In order to reduce the burden of CPU, DMA mechanism is used to transfer audio data. TMS320VC5416 has six independent programmable DMA channels. The source address register DMSRO, destination address register DMDST, unit count register DMCTR, synchronization event and frame count register DMSFC, and transmission mode control register DMMCR are used to read the data converted by pcm3008. For example, DRR11 (41h) of mcbsp1 channel is selected as the first address of DMA transmission data, and the source address is selected. In order to realize the combination of DMA and MCBSP, the DMA channel synchronization event MCBSP1 receive event is selected as DMA synchronization event. The data converted by PCM3008 is sent to the internal receiving register DRR11 of TMS320VC5416 according to the setting of MCBSP1, and then DMA reads the data in DRR11 to the specified data storage area to complete the data acquisition. When DMA transfers external data, it will

not affect the normal operation of CPU. When DMA collects the specified number of data, it will generate a DMA interrupt event to interrupt CPU to inform CPU to process it accordingly. At this time, DMA can continue to collect the next group of data according to the setting, realizing the parallel operation of data acquisition and CPU processing. The block diagram of clock management module is shown in Fig. 3 below:
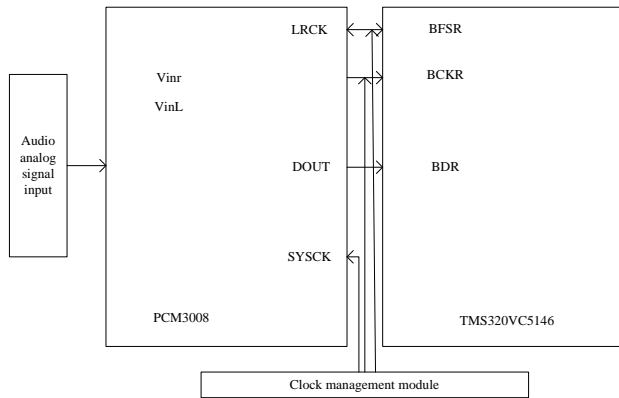

Fig. 3 Block diagram of clock management module

III. SOFTWARE DESIGN

A. Information resource search

Grid computing resources are massive, dynamic and changeable. How to search for excellent resources in the overall resources at the minimum cost is a problem in itself. In this paper, the locality principle, the working principle of cache storage system, Ant- algorithm and genetic algorithm are used to solve this problem. The basic idea of universal search algorithm in computer: local existence. Similarly, there is also a local phenomenon in grid resource scheduling. Those resources with reasonable price and good service quality may be used frequently; on the contrary, some resources are ignored. This shows that it is not ideal to search resources randomly in resource scheduling. We can start from those resources that are often used, which can achieve better results. So, we can get some inspiration from ant colony algorithm on how to establish resource fast table and what strategy to use to update resource fast table. The ant colony has several paths from its own hole to the food, but in these paths, the ant colony does not take every path, and the ant colony always chooses the shortest one. That is to say, when the ant colony chooses the path, it also has the local phenomenon. It does not choose the path with the average probability. The reason why the ant colony can do this is because of the

pheromone of the ant colony. The ant colony chooses the path according to the pheromone. The shorter path leads to more ants and higher concentration of pheromone. The ant colony is to choose the path with larger pheromone, so that all ant colonies gradually walk on the shortest path [16-21]. According to the principle of ant colony algorithm, the resources that are often scheduled are the same as the paths that are often passed by ants. Pheromones in ant colony algorithm can be introduced into the resources that are scheduled. At the beginning, ants are scattered on each resource, that is, pheromones are added to each resource, and the pheromones of each resource are updated according to the situation of resource being called. According to the size of pheromone, we can build a resource fast table, and add the resource with large pheromone to the resource fast table. If a resource with larger pheromone is successfully scheduled, it is used to replace the resource with the smallest pheromone in the resource fast table. This strategy can effectively update the resource fast table. If we choose the initial population in the resource fast table instead of randomly choosing the initial population, it will help to maintain the diversity of the population, accelerate the convergence, and greatly improve the performance of the algorithm. The resource in the resource fast table can take a certain probability as the initial population individual, and the ant in the resource fast table determines the probability that the resource is selected as the initial population individual according to the current pheromone value of each resource. The initial population is selected from the resource fast table, and the coarse-grained parallel genetic algorithm is used to make it go through several generations of evolution. The evolution space of coarse-grained parallel genetic algorithm is the whole resource space. After the evolution, the optimal solution is selected from the set of optimal values, and the resource fast table is updated.

B. Ant colony algorithm principle

Ant colony algorithm (ACO) is another heuristic search algorithm applied to combinatorial optimization problems after meta heuristic search algorithms such as simulated tardiness algorithm, genetic algorithm, tabu search algorithm and artificial neural network algorithm. Ant colony algorithm can not only search intelligently and optimize globally, but also has the characteristics of robustness, positive feedback, distributed computing and easy to combine with other algorithms. Using the positive

feedback principle, the evolution process can be accelerated; distributed computing makes the algorithm easy to be implemented in parallel, continuous information exchange and transfer between individuals, which is conducive to finding a better solution and is not easy to fall into local optimum; the algorithm is easy to combine with a variety of heuristic algorithms, which can improve the performance of the algorithm; due to strong robustness, it is based on the basic ant colony algorithm model It can be used for other problems. Therefore, the emergence of ant colony algorithm provides a powerful tool for many fields to solve complex optimization problems. When the ant completes a cycle, the pheromone concentration on the corresponding edge must be updated to imitate the characteristics of human memory and weaken the old information. At the same time, the latest information of ant access path must be summarized as follows:

$$\tau_{ij}(t+n) = \rho \cdot \tau_{ij}(t) + \Delta\tau_{ij} \qquad (1)$$

In formula (1), τ_{ij} is the number of artificial ants, t is the time, ρ is the pheromone.

The higher the total cost of the ant's path, the lower the pheromone concentration on the unit path. It's clear that ants don't release pheromones on paths they haven't experienced. The following formula is the probability of transfer to another location:

$$R = \frac{\left[\tau_{ij}(t)\right]^{\alpha} \cdot \left[\eta_{ij}\right]^{\beta}}{\sum\left\{\left[\tau_{ik}(t)\right]^{\alpha} \cdot \left[\eta_{ik}\right]^{\beta}\right\}} \qquad (2)$$

In formula (2), α, β and represent parameters respectively, and η_{ik} represent the importance parameter of information.

C. Resource information exchange

In resource scheduling, finding the best quality resources from massive resources is a time-consuming and laborious work. Therefore, we can start from those frequently used resources to improve the self selected search speed. Suppose there is a large enough resource fast table to record the information of the successfully scheduled resources, and the search for resources can start from the fast table. The computational resource search model is
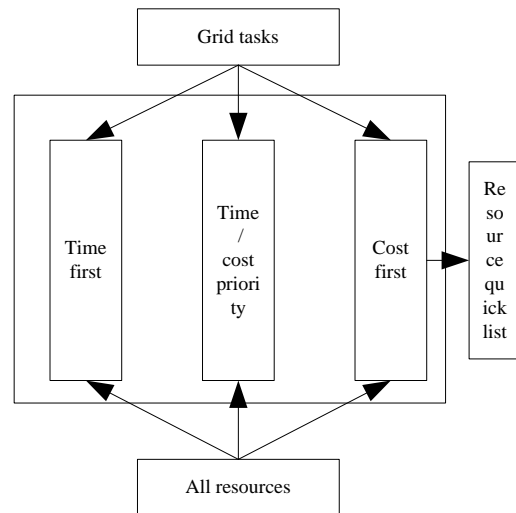
shown in Fig. 4 below:

Fig. 4 Computing resource search model

Suppose that the resource fast table is divided into three parts: the optimal time reflects the strongest computing power of resources in the fast table, the optimal cost reflects the lowest resource cost in the fast table, and the optimal time / cost uses some strategies to ensure that the resources in the resource fast table can take advantage of both time and cost. Grid computing resources are dynamic and changeable, while the programs in cache storage system are static and unchangeable. Therefore, the principle of cache storage system cannot be copied. Ant algorithm has been proved to be very dynamic. If there are large obstacles on the ant's route, the ants will find another shortest path soon, which shows the local dynamic of ant algorithm. According to the principle of ant colony algorithm, the resources that are often scheduled are the same as the paths that are often passed by ants. Pheromones in ant colony algorithm can be introduced into the resources that are scheduled. At the beginning, the pheromone is added to each resource, and the pheromone of each resource is updated according to the resource being called. According to the size of pheromone, we can build a resource fast table, and add the resource with large pheromone to the resource fast table. If a resource with larger pheromone is successfully scheduled, it is used to replace the resource with the smallest pheromone in the resource fast table. This strategy can effectively update the resource fast table. Combining the dynamics of Ant-algorithm with the dynamics of grid resources, the principle of Cache storage system can be fully used in this paper. This paper combines the dynamics of ant colony algorithm with the dynamics of grid resources, and makes

full use of the principle of cache system to improve the efficiency of resource information exchange. This is because the ant colony algorithm will adopt distributed computing in the search process, and multiple individuals will perform parallel computing at the same time, which can greatly improve the computing power and operation efficiency of the algorithm [22].

D. Implementation of information scheduling

Ant-algorithm and locality principle are only auxiliary functions in the search algorithm in this paper. Genetic algorithm plays a key role in searching resources. The combination of Ant-algorithm and genetic algorithm greatly improves the search efficiency of the algorithm, overcomes the shortcomings of genetic algorithm such as "premature" and slow convergence speed, and optimizes the performance of genetic algorithm.

One of the goals of this paper is to find as many excellent computing resources as possible at the minimum cost. We have discussed the use of ant- algorithm and Cache storage system principle to propose a computing resource scheduling model. Next, we discuss how to search resources efficiently and quickly in this model. If we choose the initial population in the resource fast table instead of randomly choosing the initial population, we can overcome the premature problem of genetic algorithm, accelerate the convergence, and greatly improve the performance of the algorithm. The resource in the resource fast table can take a certain probability as the initial population individual, and the ant in the resource fast table determines the probability that the resource is selected as the initial population individual according to the current pheromone value of each resource. The initial population is selected from the resource fast table, and the coarse-grained parallel genetic algorithm is used to make it go through several generations of evolution. After the evolution, the ideal solution is selected from the optimal value set, and the resource fast table is updated. The algorithm in this chapter is an improvement of the common coarse-grained parallel genetic algorithm.

Ant colony algorithm design, ant colony algorithm with positive feedback, collaborative and implicit parallelism makes it suitable for distributed systems, and its scalability makes it very suitable for grid environment with dynamic network structure change. When a new computing resource is added to the grid, it needs to provide its basic parameters

when the network is in good condition, the scheduling manager initializes the pheromone of the resource accordingly:

$$\tau_j(0) = \sum \frac{F_i}{P_i} \tag{3}$$

In formula (3), F_i is the MIPs of the i th processor; P_i is the resource price of the i th processor; that is, the initial pheromone of the resource reflects its inherent computing power and resource price. When a task is assigned to a resource, if the task is successfully completed, the pheromone of the corresponding resource will change accordingly, then:

$$\tau_j^{new} = \rho \cdot \tau_j(0) + \Delta\tau_j \tag{4}$$

In formula (4), ρ is the persistence of pheromone.

In this way, according to the completion of the task, the pheromone of the corresponding computing resources changes, and the resource fast table also changes. It is expressed as:

$$P_j^k = \frac{\left[\tau_j\right]^\alpha \cdot \left[\eta_j\right]^6}{\sum\limits_n \left[\tau_i\right]^\alpha \cdot \left[\eta_i\right]^\beta} \tag{5}$$

In formula (5), P_j^k represents the probability of being selected as an individual of the initial population, τ_j is the pheromone concentration of the calculated resource, η_j represents the inherent attribute of the resource, α represents the importance of the pheromone, and β represents the importance of the inherent attribute of the resource.

In order to complete the information scheduling through the above process.

IV. EXPERIMENTAL COMPARISON

In order to verify the effectiveness of the similar information scheduling system of large-scale speech recognition resources based on grid computing, the systems in Du et al. [2] and Zhao [3] are used for comparative experiments. The application effects of the three systems

are as follows.

Firstly, the information scheduling time of the three systems is compared, and the results are shown in Fig. 5 below:
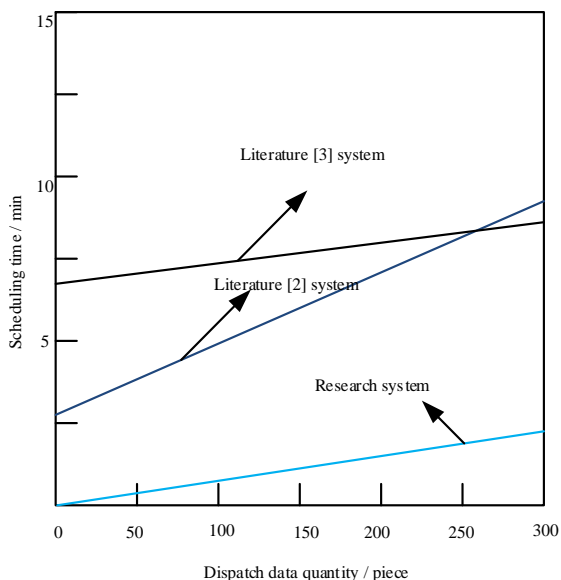

Fig. 5 Comparison of information scheduling time

In order to further verify the effect of the designed system, the information scheduling accuracy of the three systems is compared again, and the comparison results are shown in Fig. 6 below:
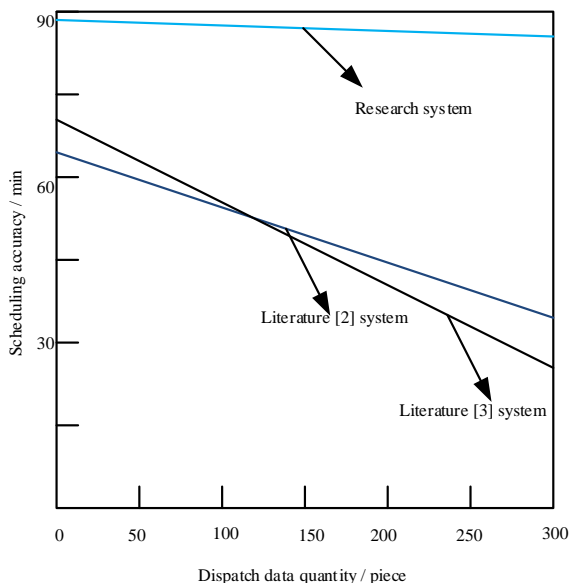

Fig. 6 Comparison of information scheduling accuracy

V. DISCUSSION

The following two conclusions can be obtained from Figs. 5 and 6, as follows:

(1) As can be seen from Fig. 5, the information scheduling time of the three systems increases with the increase of the amount of data. However, compared with the other two systems, the information scheduling time of the system designed in this paper is shorter, with a maximum of only 2.4min, while the information scheduling time of the other two systems is up to 9min and 8min, which can prove that the design method has faster information scheduling efficiency.

(2) As can be seen from Fig. 6, although the information scheduling accuracy of the three systems tends to decline with the increase of the amount of data, compared with the other two systems, the information scheduling accuracy of the design system is higher, up to 90%, which can prove that the design method in this paper can not only ensure the information scheduling speed, but also ensure the information scheduling accuracy.

To sum up, it can be proved that the design system has good resource scheduling effect, which verifies the effectiveness of the system designed in this paper to a certain extent.

VI. CONCLUSION

In order to improve the effect of large-scale speech recognition resource scheduling, a large-scale speech recognition resource scheduling system based on grid computing is designed in this paper. In the hardware part, microprocessor, Ethernet control chip, controller and acquisition card are designed. In the software part of the system, it mainly carries out the retrieval and exchange of information resources, so as to realize the information scheduling of the same type of large-scale speech recognition resources. The experimental results show that the information scheduling time of the designed system is short, the maximum is only 2.4min, and the scheduling accuracy is high, up to 90%. Through the research of this system, the efficiency and accuracy of information scheduling can be effectively improved, which has practical application significance. However, due to the lack of verification in more aspects in the research process, design research needs to be carried out next to further improve the effectiveness of the design system.

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