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Performance Evaluation of Datapath designs using FinFET and MOSFET

[1]Raju Hajare,
Department of Electronics and Telecommunication Engineering,
BMS Institute of Technology and Management, Yelahanka, Bangalore-64, Karnataka, India

Abstract: The VLSI Technology has been progressing significantly and the circuits which consume less power become major concern factor for designing todays ICs for Microprocessors and other various systems components. The Datapath is important part of a system. Adders, multipliers, and shift registers are the major components of data path unit of ALU. Almost all digital circuits and chips are made of MOSFET as the basic switching element. But same MOSFET suffers due to Short Channel Effects (SCEs) when scaled down to nano regime, which has promoted multigate device called FinFET. And this FinFET device overcomes the SCEs at technology nodes. In this paper 28T and 16T MOSFET and FinFET based full adders are designed. Using adders, 4x4 array multiplier is designed using both MOSFET and FinFET technology along with it Serial in Serial out shift register designs. The circuits designed based on MOSFET and FinFET are analyzed in terms of power and delay at various nodes. From the software characterization and analysis, it is understood that FinFET based circuits promise better performance at lower technology nodes like 22nm and 14nm than higher technology nodes in MOSFET like 250nm, 180nm, 90nm and 45nm. Hence FinFET becomes a promising device for future IC technology.

Keywords: Full Adder, Multiplier, Shift Register, FinFET, MOSFET

I. INTRODUCTION

The past four decades MOSFET has ruled the IC industry and has been scaled down to lower nodes, giving better performance upto 45nm size. This scaling trend has enabled in creating smaller and faster digital systems. However bulk CMOS scaling is facing many challenges due to material and process technology limits [1-2].The popularity and smart portable electronics is driving designers to strive for small silicon area and higher speeds and reliability.

Full adders are fundamental units in performing arithmetic operations in comparators, parity checkers, and so on [3-6].

Full adder circuits are in critical paths of complex arithmetic circuits for multiplication and division. And these in turn influence the overall performance of the system. Adder is vital component of CPU, ALU and floating-point units. Here various designs of adder have been carried out using MOSFET and FinFET and evaluated the results. These adders are extensively used in data path designs with care taken while designing the system to achieve optimum performance. The array algorithm used in simple addition and shifting operation consist of logic gates like AND gates and adders [7-10].

The advantage of array multiplier is its regular structure, that helps in easy layout designs in VLSI. This regular layout structures are widely used in VLSI math co-processors and DSP processor chips [11-14]. Shift register used in digital circuits is nothing but cascade of flip flops sharing the same clock. Here output of each flip flop is connected to data input of next flip flop in the chain [15-18]. This paper aims at designing adder, multiplier and shift register using devices FinFET and the Conventional MOSFET for different technology nodes using tool HSPICE.

Using net list of both devices, circuit performance of the both the FETs are analyzed. The work here emphasizes on the important parameters such as speed, power, and size in case of processors [19-21]. It is proposed here to optimize size of device, reduce the delay and power dissipation, considering Predictive Technology Models files. Adder is implemented using different logic style like pass transistor and transmission gate logic. In the proposed work, adder,

multipliers, and shift register designs are explored with above said parameters [22-23].

A. Full adders: As full adder is main block of data path in an ALU of processor architecture, we have evaluated the performance of Full adders using both devices. The table 1 shown below is for full adder circuit using 28T MOSFETs and evaluation is done in terms of power and delay.

Table 1: Results of full adder cell using 28T MOSFETs

Technology node	Power (Avg)	Power (Max)	Delay (Sum)	Delay (Carry)
250nm	23.68 µ	1.79m	211.77ps	136.26ps
180nm	6.566 µ	557.94 µ	176.12Ps	112.16Ps
90nm	1.199µ	158.94 µ	66.30Ps	45.61Ps
45nm	27.33m	27.43m	failed	failed

Table gives the values for various parameters such as power and delays, when evaluated full adders built using 28T MOSFETs. And 45nm and below the device fails to give the results due to its Short Channel Effects (SCEs) and further it is not possible to evaluate device performance. Therefore, new novel device called FinFET based 28T full adders' circuits are built at 32nm, 22nm and 14nm and performance has been evaluated.

Table 2: Results of 28T FinFET based full adder cell

Technology node	Power (Avg)	Power (Max)	Delay (Sum)	Delay (Carry)
22nm	61.15n	26.72µ	30.84p	24.76p
14nm	31.15n	25.23µ	19.33p	18.65p

Table 2 contains the values for average and maximum power and delays for 28T FinFET based full adder circuit with improvement in the performance of the circuit giving low power and smaller delay values.

Similarly, full adder circuits using MOSFETs evaluated as shown in Table 3.

Table 3: Results of Full adder cell using 16T MOSFETs

Technology node	Power (Avg)	Power (Max)	Delay (Sum)	Delay (Carry)
250nm	17.06µ	1.99m	23.65p	3.68p
180nm	3.648	549.94µ	21.52p	3.24p
90nm	2.17µ	196.14µ	15.01p	2.61p
45nm	1.89µ	90.95µ	3.54p	1.25p

Above table 3 gives values for full adder design using 16T MOSFET.

The results for 16T FinFET based adder circuits at 22nm and 14nm is analyzed as in table 4.

Table 4: Results of full adder cells using 16T FinFETs

Technology node	Power (Avg)	Power (Max)	Delay (Sum)	Delay (Carry)
22nm	30.15n	19.72µ	10.84p	2.116p
14nm	19.75n	10.43µ	8.93p	2.065p

From the Table 4, it is inferred that FinFET based full adder circuit gives improvement in the results at 22nm and 14nm node technologies. Thus, 16T FinFET based Full Adder circuit outperform compared to MOSFET based adder circuits. Therefore, FinFET is better replacement for MOSFET devices in future ICs [22].

II. ARRAY MULTIPLIERS

Generally, multipliers are found as basic blocks in various processing units including signal processing, communication systems and instrumentation. Multiplier application also include mixers, neural networks implementation.

The array multipliers of 28T MOSFET and FinFET are evaluated at different node technologies. Table 5 shows the results for 28T MOSFET based array multiplier and Table 6 shows the results for 16T MOSFET based array multiplier respectively.

Table5. Results of 28T full adder based **MOSFET** array **multiplier**

Technology node	Average power (W)	Maximum power(W)	Average Delay(s)
250nm	58.7142u	10.3314m	2.0703n
180nm	12.7370u	2.7726m	1.9701n
90nm	5.1511u	2.5388m	1.8091n
45nm	328.9834m	330.4205m	Failed

Table 6: Results of 16T Full Adder based MOSFET array multiplier

Technology node	Power (Avg)	Power (Max)	Delay (Avg)
250nm	45.7105u	6.6924m	2.0078n
180nm	8.7845u	2.2329m	1.9297n
90nm	4.8381u	2.3778m	1.8010n
45nm	37.3893m	1.5411m	Failed

It is clear from the table shown above is that there is a increase in the values for power and delay parameters in 16T MOSFET based multiplier at 45nm node and below that due to SCEs.

A. 28T FULL ADDER BASED FinFET ARRAY MULTLIPLIER

A.2(a): 22nm Node, V_{dd}=0.9v

Results: Average power= 1.1618uW

Maximum power= 546.3083uW, Average delay=47.4271ps

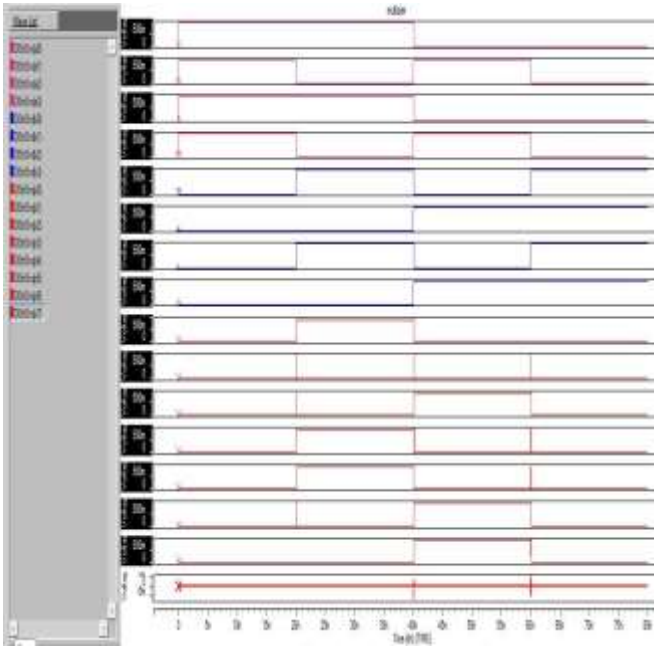

Fig 3.2(a): 28T Full adder based FinFET Multiplier output waveform at 22nm

A.2(b): 14nm Node, V_{dd}=0.8v

Results: Average power=1.2358uW

Maximum power= 404.3780uW, Average delay= 27.8449ps

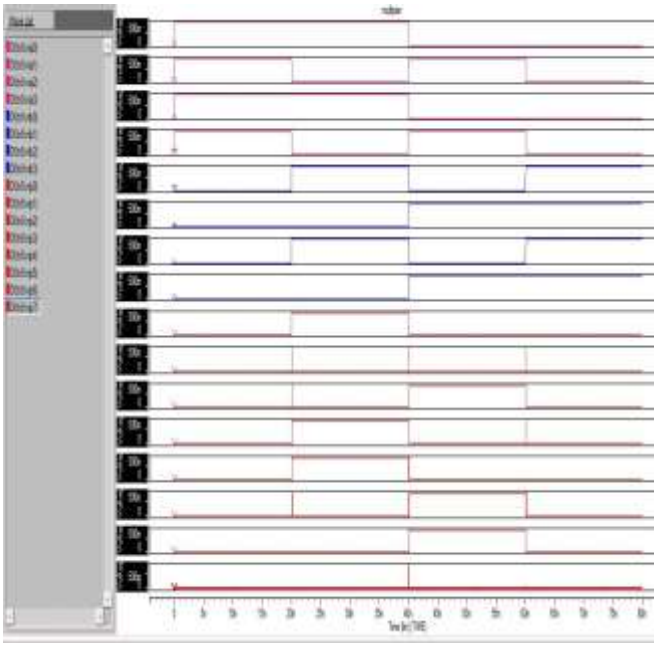

Fig 3.2(b: 28T Full adder based FinFET Multiplier output waveform at 14nm

The figure 3.2(a) and 3.2(b) gives the resultant waveform of 28T full adder-based array multiplier at 22nm and 14nm

respectively. From the graphs we can analyze and conclude that FinFET based multiplier circuit give better performance in terms of dalay and power compared to MOSFET based multiplier circuits. Observations from the waveform are noted in the following table 7.

Table 7: Results of 28T Full Adder based **FinFET** array **multiplier**

Node	Average power (W)	Maximum power(W)	Average Delay(s)
22nm	1.618u	546.3083u	47.4271p
14nm	1.2358u	404.3780u	27.8449p

Result table contains the power and delay values for FinFET based 28T full adder multiplier. And we can observe that both power and delay values are reduced with FinFET based multiplier circuit. Compared to MOSFET based multiplier.

B. 16T FULL ADDER BASED FinFET ARRAY MULTIPLIER

B.(a): 22nm Node, V_{dd}=0.9v

Results, Average power= 1.1618uW

Maximum power=546.3083uW, Average delay= 4.9005ps

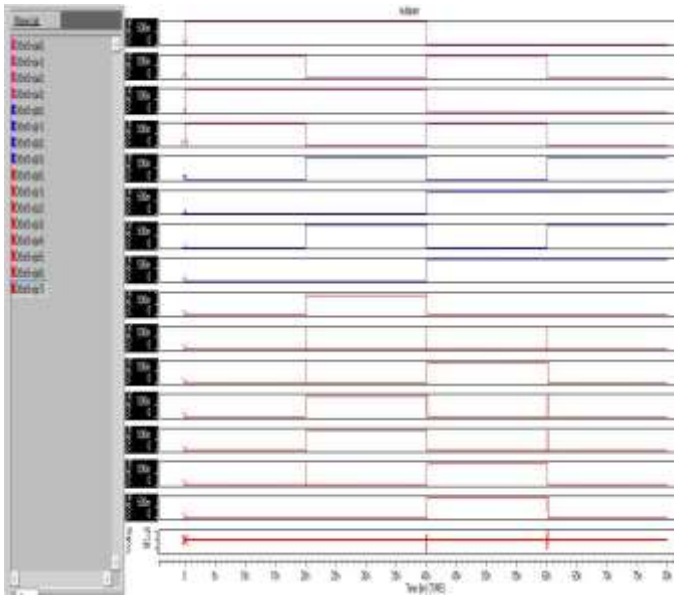

Fig 3.3(a): 16T Full adder based FinFET Multiplier output waveform at 22nm

B. (b): 14nm Node, V_{dd}=0.8v

Average power= 219.8364nW

Maximum power= 241.7477uW, Average delay= 38.2305ps

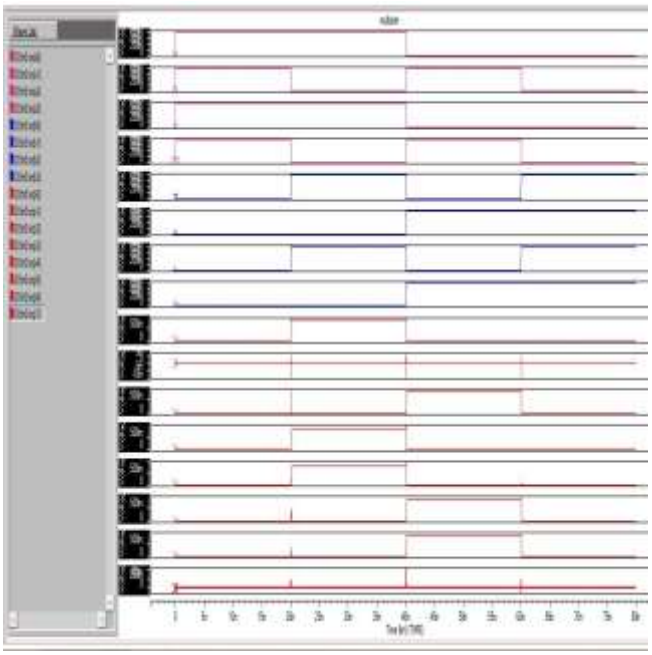

Fig 3.3(b): 16T Full adder based FinFET Multiplier output waveform at 14nm

The figure 3.3(a), 3.3(b) gives the resultant waveform of 16T full adder-based array multiplier at 22nm and 14nm respectively. From the graphs it is clear that FinFET based multiplier gives better results in terms of behavior and performance than MOSFET based multiplier at lower nodes.

Table 8: Results of 16T Full Adder based FinFET array multiplier

Technology node	Power (Avg)	Power (Max)	Average delay(s)
22nm	370.7442n	366.1094u	64.9005p
14nm	219.8364n	214.7477u	38.2305p

From the above simulated results and table which contains the power and delay values for 16T full adder based FinFET array multiplier we can conclude that FinFET is a better replacement for MOSFET devices.

III. MOSFET BASED SHIFT REGISTER

A.1(a): 90nm Node, V_{dd} =1.5v

Results: Average power=10.9377uW

Maximum power= 606.6281uW,

Delay=22.1268ps

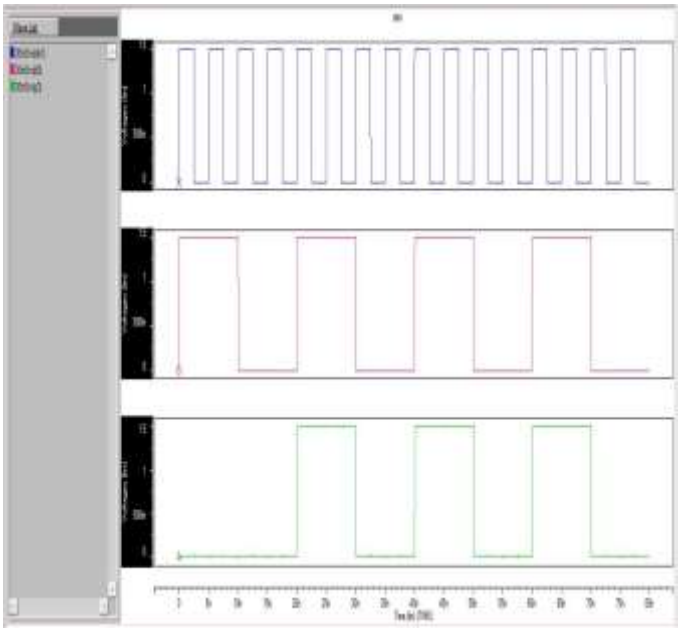

Fig 4.1(a): MOSFET based shift register output waveform at 90nm

A.1(b): 45nm Node, V_{dd}=1.2v,

Results: Average power= 60.8975uW

Maximum power=370.7403uW, Delay Failed

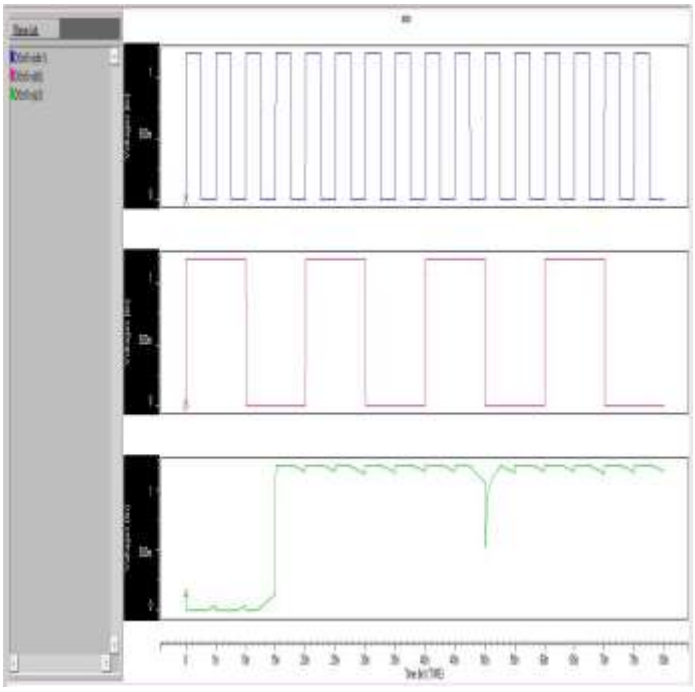

Fig 4.1(b): MOSFET based shift register output waveform at 45nm

The delay and power is calculated at 250nm, 180nm, 90nm and 45nm also as shown in the table 9. But figures 4.1(a), 4.1(b), gives the resultant waveform of MOSFET based shift register at 90nm, 45nm respectively. The results of MOSFET based shift register are tabulated as below in table 9.

Table 9: Results of MOSFET based Shift Register

Technology Node	Power (Avg)	Power(max)	Delay (Avg)
250nm	77.0716u	5.2178m	53.6090p
180nm	19.5625u	1.1352m	41.5581p
90nm	10.9377u	606.6281u	22.1268p
45nm	60.8975u	370.7403u	Failed

From above values it is clear that the MOSFET based shift register circuits suffer below 45nm due to SCEs.

B. FinFET BASED SHIFT REGISTER

B.(a): 22nm Node: V_{dd}=0.9v

Results: Average power=437.1818nW

Maximum power=62.1376uW, Delay=14.1734ps

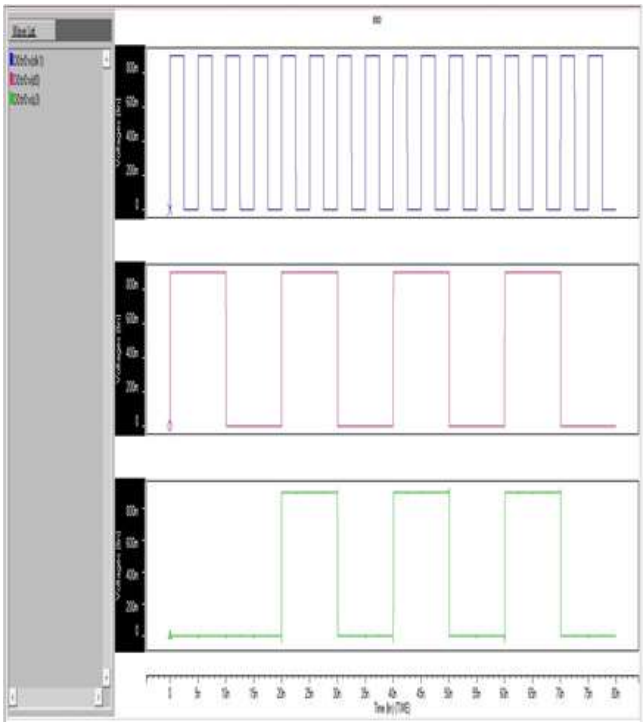

Fig 4.2(a): FinFET based shift register output waveform at 22nm

B.2.(b): 14nm Node: V_{dd}=0.8v

Results: Average power=267.5868nW

Maximum power=52.4975uW, Delay=9.0458ps

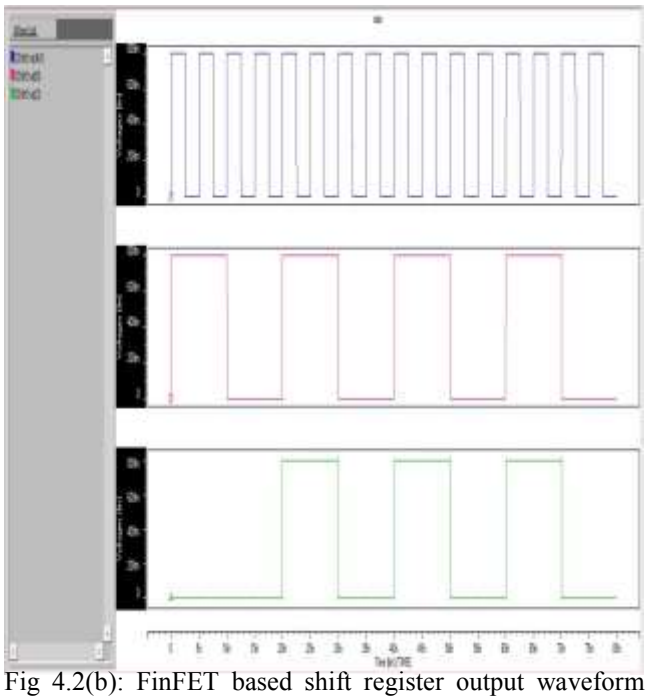

Fig 4.2(b): FinFET based shift register output waveform at 14nm

The figure 4.2(a), 4.2(b) gives the resultant waveform of FinFET based shift register at 22nm and 14nm respectively. From the graphs we can analyze that replacement of MOSFET by FinFET in shift register gives better results in terms of its power and delay, enhancing the performance compared to MOSFET based shift register at lower technology nodes.

Table 10: Results of FinFET based Shift Register

Node tech	Average power	Maximum power	Average Delay(s)
22nm	437.1818n	62.1376u	14.1734p
14nm	267.5868n	52.4975u	9.0458p

From the above table shown, it is observed that power and delay values for FinFET based shift registers at 22nm and 14nm nodes are favorable compared to MOSFET based circuit. Hence FinFET based shift register circuits have upper hand and it is a better choice at lower technology nodes

IV. CONCLUSION

From the work carried out here, conclusion can be drawn that 28T and 16T MOSFET and FinFET based full adders were designed and evaluated for the performance.

It is observed that 16T FinFET based full adder gives 48% and 25% improvement in power and delay parameters respectively when compared to 28T FinFET based full adder.

4x4 array multipliers are designed using both 28T and 16T full adders. From the evaluated results it is analyzed that the 16T full adder based 4x4 array multiplier gives 20% improvement in power compared to 28T full adder based 4x4 array multiplier. Also Shift register has been designed using D flip flops with FinFET and MOSFET technology nodes.

Our observation shows that FinFET based shift register gives favorable results compared to MOSFET based shift register with 18% improvement in power and delay.

Finally, from the software characterization of data path(Adder, Multiplier and Shift Register)circuit it can be cconcluded that the FinFET based circuits outperform when compared to bulk MOSFET based circuits at nano regime.

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