INTERNATIONAL JOURNAL OF CIRCUITS, SYSTEMS AND SIGNAL PROCESSING
DOI: 10.46300/9106.2022.16.110 Volume 16, 2022

Miller's Compensation Techniques for a High Gain, High BW OP-AMP at 65 nm Technology

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Received: March 15, 2021. Revised: February 17, 2022. Accepted: March 6, 2022. Published: March 28, 2022.

Abstract— **OP-AMPs find applications in different domains of electronics engineering including communications. There have been several OP-AMP configurations realized in the last decades for different target applications. But with the evolution of communication standards, to meet the demand for high data rate over the years, the requirement for a high frequency and high BW OP-AMP is gaining attention. This makes the design challenge much higher. This paper presents a two-stage CMOS amplifier that uses a frequency compensation method to facilitate higher BW. Different parameters like Gain, Gain bandwidth product (GBWP), Phase Margin, and Total Power dissipation are considered in this design. A step-by-step procedure for an efficient amplifier design is followed using frequency compensation. We have achieved a gain-bandwidth product (GBWP) of 110 MHz that is capable of driving large capacitive loads. It also achieves 77.7 dB gain and phase margin of 60° with the minimal noise of 2.27 $\mu V/\sqrt{Hz}$ and the slew rate of $20.12\ V/ms$.**

Keywords—Compensation, Gain Bandwidth product

I. Introduction

OP AMPs are the basic building blocks of many electronic applications. Communication is a domain where it plays a very vital role in signal conditioning. Though different OP-AMPs are being designed over the years but with the advancement of a communication standard, design challenges are also going up. OP AMPs need to be optimized to be used in analog systems to facilitate higher accurate gain, input and output impedance matching, line development, and bandwidth expansion.[1][2] Apart from the other challenges, the biggest challenge is to improve op-amp stability in the wide bandwidth. The solution is therefore to compensate the magnifier according to the frequency response process.

The purpose of this paper is to design a simplified frequency compensation scheme along with the OPAMP to make it stable with high gain in high frequency range. Secondly the proposed circuit must have the less power consumption and generate less noise so the second problem is to make the design power aware and noise aware. For this we will use a two stage Miller compensation circuit.

This paper presents a two-stage CMOS amplifier which uses frequency compensation method to facilitate higher BW. Different parameters like Gain, Gain band width product (GBWP), Phase Margin and Total Power dissipation are considered in this design. A step-by-step procedure for an efficient amplifier is followed using frequency compensation. We have achieved a gain-bandwidth product (GBWP) of 110 MHz that is capable of driving large capacitive loads. It also achieves 77.7 dB gain with a phase margin of 60° with the minimal noise of 2.27 $\mu V/\sqrt{Hz}$ and the slew rate of $20.12\ V/ms$.

The remaining part of the paper is organized as follows. Section II describes the circuit fundamentals, section III describes the principle of frequency compensation technique and its importance, section IV deals with mathematical calculations. Section V presents the simulation results and the improved circuit design with its results and the comparison with the previous circuit and lastly, section VI includes concluding remarks.

II. Fundamentals of the Proposed Circuit

A. Two-stage Miller,s Compensation

The block diagram is shown in the figure below.

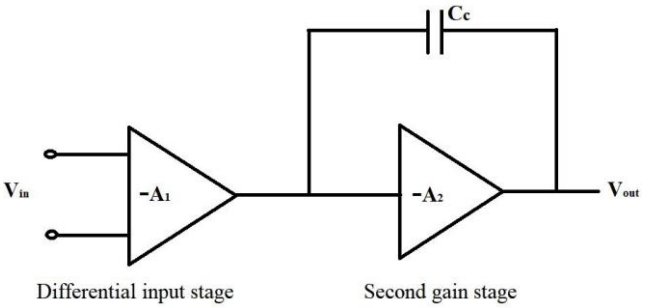

Fig. 1 Block diagram of a Miller compensated operational amplifier

It is basically a two-stage frequency compensation circuit where the two stages can be modeled as the cascade of two amplifiers. Here the first stage is a differential amplifier that acts as an input differential pair and also it forming a current mirror circuit acting as a load. The second stage is the common source stage which acts as a gain stage. The need for this common source arises for the gain obtained from the differential amplifier is not high enough. The compensation capacitor is connected to the second stage to shift the associated transmission zero to a higher frequency. The Miller-effect of a bug and more of the dominant, the second part of the pole down in frequency, while the other, less dominant, and the sign of the pile-up in the frequency of post-distribution). This action is intended to ensure a good phase margin, the force of the transfer function of the system is to act as a single-pole system. The Miller compensation method is that there is a compensation capacitor is to be installed

between the initial level of output (differential amplifier), and the op-amp output gain: the output of the amplifier).

A two-stage amplifier can be modelled as a cascade of two amplifiers as shown in Figure 2. The first stage is a differential amplifier, which generates an amplified version of the difference input signal. In this stage, the CMRR, slew rate, and other characteristics are to be determined.

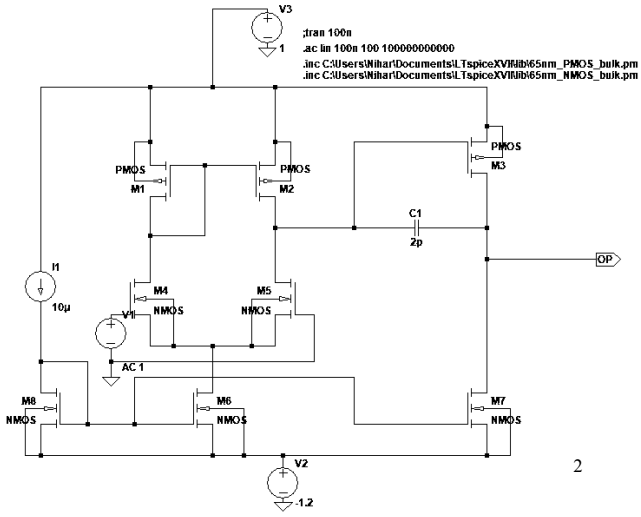

Fig. 2: Miller compensated two stage operational amplifier

The second stage is an inverting amplifier. The purpose of this step is to ensure that a large current gain. The gain stage and the input stage forms two poles which have impact on the stability of the feedback system. Compensation techniques needs to be used in order to ensure the stability of the amplifier in a specific gain.

The design consists of a NMOS differential amplifier with an active load for the first stage, and a PMOS common-source amplifier as the second stage. A compensation capacitor is connected between the second levels of the output of the first stage from the output to obtain a post-distribution, which means that, in the case of an op-amp. Here the simulation is done in LTspice at 65nm CMOS technology. For a simple two-stage op-amp, as shown in Figure 2. A standard power supply, it will also be used to generate the power for the reference only. The parts of each of these blocks will be discussed in the following sections of this document. The required operational amplifier specifications are descried below.

III. FREQUENCY COMPENSATION TECHNIQUE

Single-stage amplifiers are naturally stable and have a very good response frequency that assumes that the bandwidth of profit is ten times higher than a single pole. However, single-stage amplifiers suffer from low dc gain and are much lower than submicron CMOS transistors. Generally, Op Amps require at least two profit categories that present multiple beams in response to frequency. The poles contribute to the change of the negative phase and can cause if $\angle FA$ (phase margin) to -180° before the bonds gain frequency. Therefore due to insufficient phase value the region would change. The amplifier circuit therefore needs to be modified to increase the phase limit and tighten the closed loop circuit. This process is called "compensation". With intuition, two different methods can be taken to stabilize the loop. The most direct way to make a profit is to go down quickly so that the phase shift is less than -180° in the difficulty of gaining a single. This method gains stability by reducing the amplifier bandwidth and the highly differentiated pole separation method uses this process. Another compensation method pushes the frequency of the crossover phase by minimizing the transition to the full phase. In this particular case the total number of poles needs to be reduced while maintaining the profit of the dc. This is achieved by introducing eggs into the opening and pulling operation to close the poles, or by using feeding methods to improve the edge of the section without tying the bandwidth in a way as small as cracking a pole.

IV. MATHEMATICAL CALCULATION

A design step for two stage Op Amp can be constructed as

Basic op amp Equations are

$$I_D = \frac{\mu_{n,p} C_{ox}}{2}\left(\frac{W}{L}\right) V_{ov}{}^2 \; or \; \frac{W}{L} = \frac{2I_D}{\mu_{n,p} C_{ox} V_{ov}{}^2}$$

Trance – conductance, $g_m = \sqrt{2\mu_{n,p} C_{ox}\left(\frac{W}{L}\right) I_D}$

$$= \frac{2I_D}{V_{ov}}$$

$V_{ov} = V_{GS} - V_T$, here V_{ov} is called voltage overdrive.

Step 1: we have to design the compensation capacitor C_c

$$C_c = \frac{g_{m1}}{2\pi f_{uf}}$$

It should be noted that the compensation capacitor needs to be optimized again after the design procedure is complete. During simulation tweaking the compensation capacitor is required to obtain the appropriate stability.

Step 2: we have to calculate g_m

$$gm_{1,2} = GB \cdot C_c$$

Step 3: then we calculate $I_{D1,2}$

$$I_{D1,2} = SRC_c$$

Step 4: thus we can calculate the aspect ratio $\left(\frac{W}{L}\right)_{1,2}$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(g_m)^2}{K_n \cdot I_{D1,2}}$$

Similarly, this way we can calculate the aspect ratio for the other MOS as well.

V. Simulation Result

The circuit shown in Fig. 2 has been designed in a 0.65-µm CMOS technology. A supply voltage of ±1.5 V has been employed. The following transistor dimensions are calculated by using the equations presented in the previous section. It is expressed as W(µm)/L(µm) per transstor. M_1 ➔ 7/1, M_2 ➔ 7/1, M_3 ➔ 60/1, M_4 ➔ 3/1, M_5 ➔ 3/1, M_6 ➔ 15/1, M_7 ➔ 70/1, and M_8 ➔ 10/1. The input voltage of ±0.400 mV have been applied and the bias current of I_1 = 10µA. A conservative compensation capacitance Cc = 20 pF has been chosen for the proposed circuits.

A. Result analysis

This section presents various simulation results of electrical characteristics of two stage op amp such as transient analysis, gain, frequency analysis, and noise, power and output voltage.

1) Transient analysis

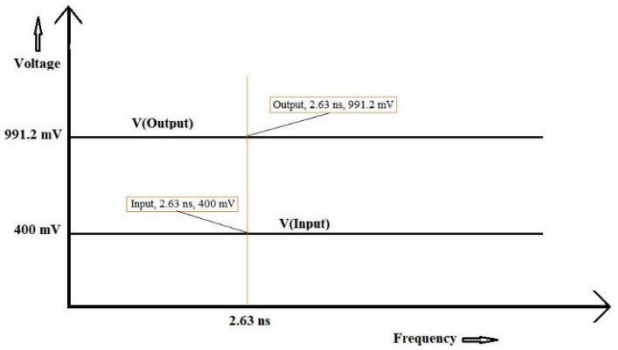

Fig. 3: Transient analysis

The Transient analysis in the time domain, it is a study of one parameter, such as voltage or current builds up in the course of time. If we look at the raw data, we can see that the behavior for a certain period of time. From this result we can see the increase in the output voltage as compared to the input. For the input voltage of 400mV we get the amplified output of 991.2 mV.

2) Frequency analysis

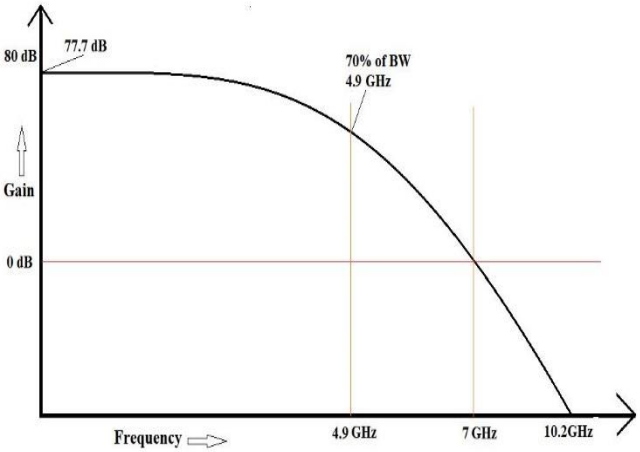

Fig. 4: Frequency analysis

The Frequency analysis presented in figure 4 shows that the design works well in higher frequency band up to around 4.9GHz. We can think of the noise in the graph in a Cartesian coordinate system with a real and an imaginary axis, we can think of it as a Nyquist diagram. From the frequency analysis we can check the frequency, BW, GBP. Here the open loop gain we get is 77.7 dB, and the bandwidth is 4.9 GHz. Thus, results in the gain bandwidth product of 110*MHz*

3) Phase Margin

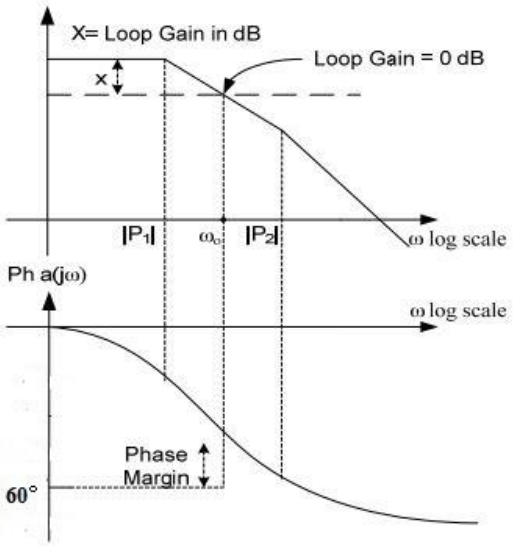

Fig. 5: Phase and gain relation

Additional phase lag that makes the system on the verge of instability is called the phase margin. Here we get the phase margin of $60°$ as shown below. The phase and gain margins are presented in figure 5 and figure 6.

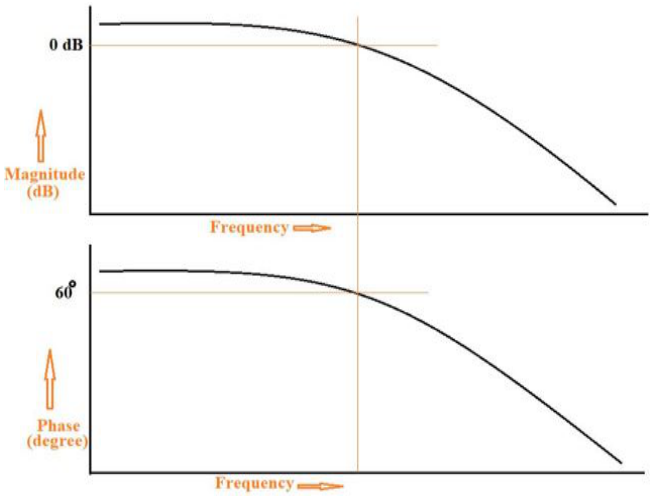

Fig. 6: Phase Margin

4) Noise analysis

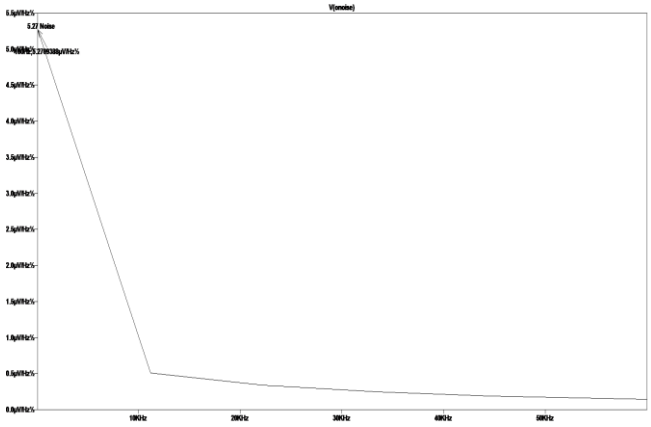

Fig. 7: Noise analysis

The noise analysis shown in figure 7 depicts that the noise level is equivalent to the system, as well as the injection of noise from an external source, in the right environment. Noise analysis in an op-amp circuit is very critical where accuracy is the prime concern. In this result we get the noise of 5.27 $\mu V/\sqrt{Hz}$.

5) Slew rate

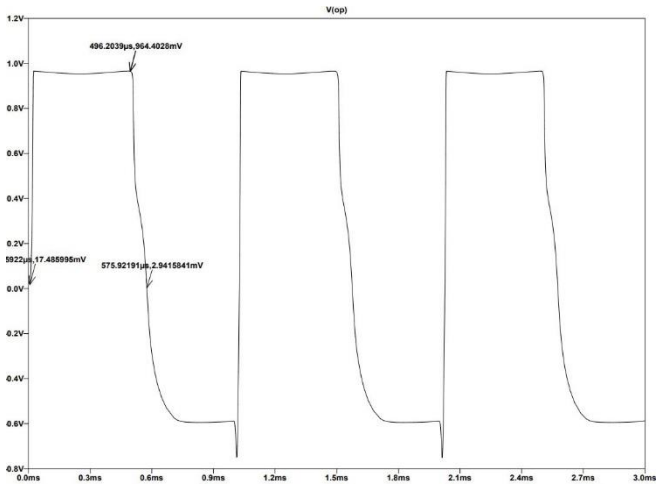

Fig. 8: Input signal

Slew rate is the maximum rate of change of an op amp's output voltage. it measured by applying a large signal step to the input of the op amp, and measure the rate of change from 90% to 10% of the output signal amplitude. Thus it can be shown as, $SR = \frac{\Delta V_{out}}{\Delta T} = \frac{V_{out90\%} - V_{out10\%}}{t_{90\%} - t_{10\%}}$. In the fig.8 shown above

$$\Delta V_{out} = V_{out90\%} - V_{out10\%}$$
$$= 771.52 \text{ mV}$$

Similarly for time also

$$\Delta Time = t_{90\%} - t_{10\%}$$
$$= 64.56 \ \mu V$$

Thus, substituting the value of ΔV_{out} and $\Delta Time$ in the slew rate expression, we get

SR = 11.95 V/ms.

B. Results Chart

Below shows the results of the proposed circuit.

Parameter	Value
Open Loop Gain	77.7 dB
Bandwidth	7 dB
Phase Margin	60°
Noise	5.27 $\mu V/\sqrt{Hz}$
Output Voltage for the input voltage of 400 mV	991.2 mV
Slew rate	11.95 V/ms
Power Dissipation	14.32 mWatt

Table 1: simulation results

The proposed circuit results in the output voltage of 991.2mV for the input of 400mV, the output of the circuit generates more than twice the input of the supply to the circuit.. Now substituting the values of the output voltage and the input voltage in the equation for voltage gain given below.

$$Voltage\ gain(A_v) = \frac{V_{output}}{V_{input}}$$

In dB, $a_v = 20 \log A_v$

Here $V_{output} = 991.2mV$

$V_{input} = 400mV$

Thus, substituting in the above equation

$A_v = 2.48$

$$In\ dB\ a_v = 20 \log A_v$$
$$= 20 \log (2.48)$$
$$= 7.89$$

Thus, voltage gain in 7.89 dB.

Since the gain is greater than one or greater than zero dB, that is amplification, and is defining property of an active circuit.

As mentioned above the design is implemented using 65nm CMOS technology and the platform used is LTspice. From the simulation result it can be clearly seen that the design

gives better output voltage with high gain and the better Gain Bandwidth Product. The circuit produce less output noise and moderate slew rate. To reduce the noise more and improve the slew rate of the circuit we have improvised the circuit which will discussed in the section C.

C. Improvement of the circuit

In the previous circuit given in fig 2 two transistor are connected at the output the circuit. The connected transistor introduced a simple voltage follower formed by transistors M9 and M10 has been the chosen implementation. This two additional MOS device forms a voltage follower circuit connected to the end of the gain stage of the circuit. The final output of the circuit is still connected in the gain stage as shown in the figure.

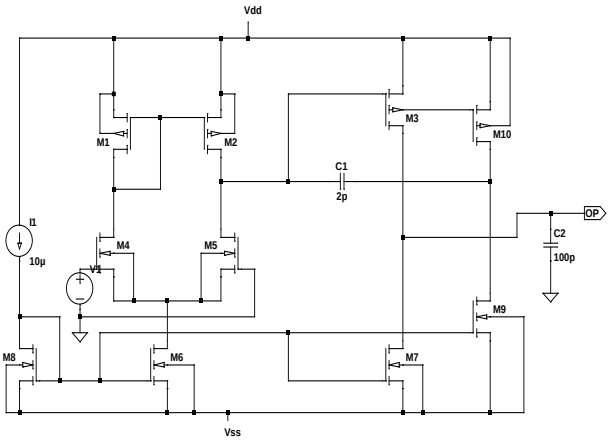

Fig. 9: Two stage operational amplifier with voltage follower

A voltage follower is an op-amp circuit whose output voltage is equal to the input voltage. Thus Voltage follower provides no attenuation or amplification but only buffering the input signal and has a voltage gain of 1. With the addition of the voltage follower circuit the noise and the slew rate of the circuit also get improved. Below shows the results of noise analysis and the slew rate of the improved circuit and their comparison with the previous circuit. This type of arrangement is simple and suitable for solving complex impedance relationships. In the event of signal transmission from a high-output impedance sub-circuit to a low-input impedance sub-circuit, then the voltage follower between these sub-circuits ensures that there is a complete voltage transfer in the load phase.

Few advantages of the voltage follower circuit are
[1] The device delivers a gain of both current and power
[2] The minimal output impedance of the circuit makes use of the output
[3] It utilizes '0' current from the input section
[4] No loading effect are there
[5] Minimal output impedance. Etc.

In this circuit the output coming from the compensation capacitor is passes to the voltage follower circuit where a PMOS of dimension of $w/l = 4\mu m/1\mu m$ and a large size of NMOS with dimension of $w/l = 100\mu m/1\mu m$.
The results of this circuit will discussed below.

1) Transient Analysis

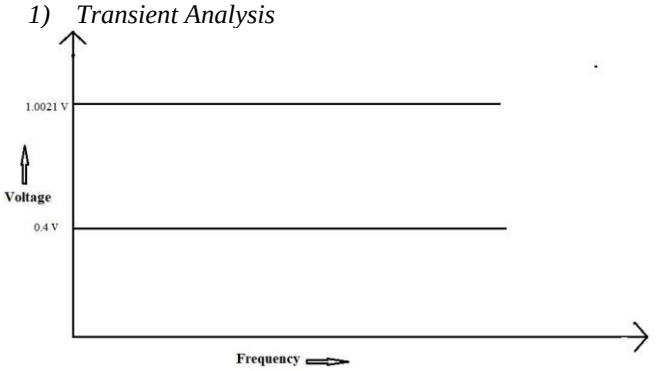

Fig. 10: Transient analysis

The circuit results the output voltage of 1.002 V for the input of 400 mV while in the previous circuit the output voltage of 991.2 mV for the input of 400 mV. Thus it can clearly see that due to the addition of that circuit voltage gain is slightly increased.

Thus, the gain will be $A_v = \frac{1.002}{0.4}$
$= 2.505$

Voltage gain in dB is 7.98 dB.

2) Frequency Analysis

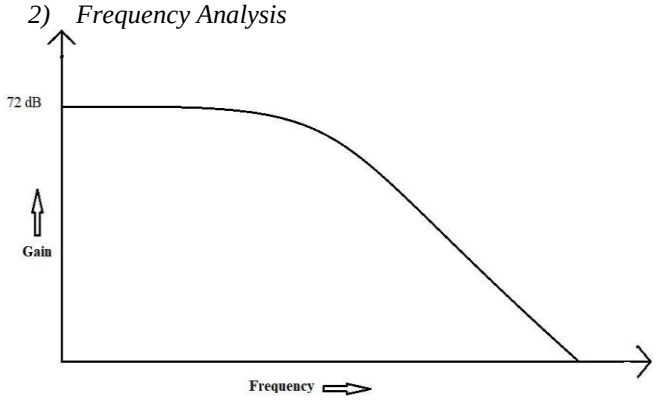

Fig. 11: Frequency analysis

In the frequency analysis here we get a little bit lower gain which is 72 dB whereas in the previous circuit we got the gain of 77.2 dB. Though gain is decreased almost by 5 dB unit but it is still in a good range era for high gain frequency analysis.

3) Noise analysis

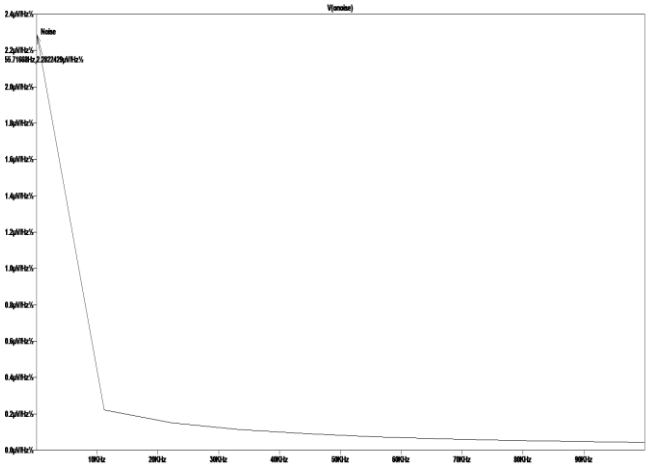

Fig. 12: Noise analysis

After connecting the voltage follower circuit the noise generated by the circuit has reduced from 5.27 $\mu V/\sqrt{Hz}$ to 2.27 $\mu V/\sqrt{Hz}$

4) Slew rate

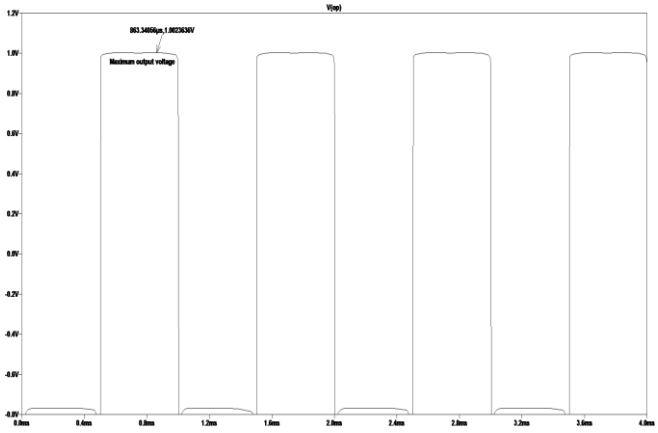

Fig. 13: Slew rate

From the figure 90% and 10% of Vout are 900mV and 100mV respectively. Similarly 90% and 10% of time t are 44.73 µV and 4.97 µV respectively.

$$Slew\ rate = \frac{(900-100)}{(44.73-4.97)}$$
$$= \frac{800}{39.76}$$
$$= 20.12\ V/ms$$

5) Power dissipation

In electronics power dissipation is a process where the devices waste some energy by producing heat as an undesirable derivatives of its primary action.

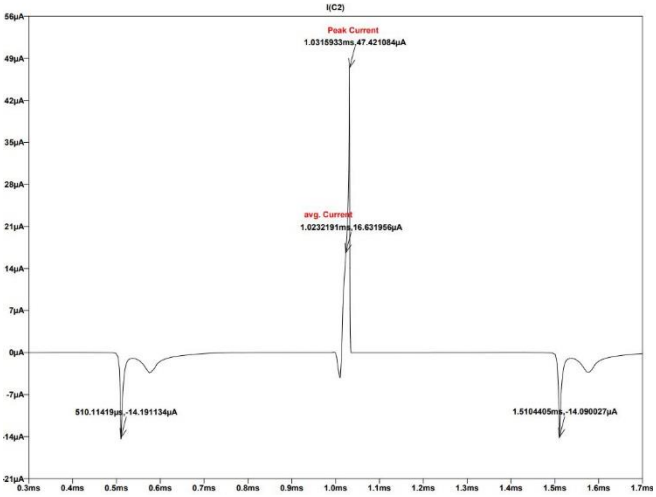

Fig. 5: Input current

The formula to find the power dissipation in a circuit is $P = I \times V$. Here both *I* and *V* are the RMS value. From the above figure 5, *I* and *V* are 21.46 µA and 681.78 mV.
Now, substituting the value in the expression

$$P = 21.46 \times 681.78$$
$$= 14.63\ mWatt$$

Thus, the power dissipation in circuit is 14.63 mWatt.

6) Comparasion with the prvious circuit

The following table shows the difference of the results for the of improved circuit with the previously proposed circuit

Parameter	Previous Circuit	Improved Circuit
Output Voltage	0.992V	1.002V
Open loop gain	77.2dB	72dB
Noise	$5.27\ \mu V/Hz^{\frac{1}{2}}$	$2.27\ \mu V/Hz^{\frac{1}{2}}$
Slew Rate	$11.95\ V/ms$	$20.12\ V/ms$

Table 2: Comparison table

D. Conclussion

The following circuit results less noise and better slew rate compared to the previous circuit just by connecting a voltage follower circuit at the output. But it has some limitations also. Since two MOS are connected additionally so the size of the circuit is also increased and need to lose some amount of gain compared to the previous one. The paragraph given below will show the comparison of this circuit with some previously done papers on this topic.

E. Comparative Tables

In this section we compare this results with some previously reported works.

Paper	Technology	Gain	PM	Noise
2017[1]	180 nm	61	68°	14 $\mu V/\sqrt{Hz}$
2018[2]	180 nm	63	78°	8 $\mu V/\sqrt{Hz}$
2019[3]	180 nm	73	56°	13.6 $\mu V/\sqrt{Hz}$
2020[4]	180 nm	70	72°	14 $\mu V/\sqrt{Hz}$
This paper	65 nm	72	60°	2.27 $\mu V/\sqrt{Hz}$

Table 2: Comparison table

VI. CONCLUSSION

This work implements a two-stage OP-AMP for high BW applications. Frequency compensation technique is successfully used to attain high BW while maintaining a sufficiently higher gain and GBWP. Different other parameters like Phase Margin and Total Power dissipation are considered in this design to make it stable and to have low power dissipation. A step-by-step procedure for an efficient amplifier design is followed. We have achieved a gain-bandwidth product (GBWP) of 110 MHz that is capable of driving large capacitive loads. It also achieves 77.7 dB gain with a phase margin of 60º. Hence this design can be claimed to be suitable for high frequency applications.

As a part of the future research, the developed two-stage amplifier, a compensation method can be extended to the implementation of a three-phase-to-phase and multi-amplifier system. The formal results and the design procedure and prior to the use of a multi-amplifier system can be developed with the aid of the frequency offset method. The frequency of the compensation method is with a low-voltage, low-power Op-amp in the correspondence and can be used to make effective, data converters, analog filters, and other signal processing units in modern sub-micron CMOS process. The method used in this study should facilitate the integration of analog circuits in modern, low- power, high-speed applications.

Some of the specific applications of this technique are

[1] 5G transmission node for the frequency band of 3.3 GHz – 3.6 GHz as per report of TRAI.

[2] High gain and high bandwidth op-amps are used in communications like in cellular telephones, antenna transmitter, wireless, LAN (WiFi), and satellite communications.

[3] Data converter circuits require fast settling and high gain amplifiers. The high gain is needed for the output of the amplifier to settle accurately to the desired final value.

[4] In a satellite communications system, the transmitting and receiving Antenna uses an high gain and high bandwidth operational amplifiers.

[5] The high gain amplifiers boosts the antenna signal to beat feed line losses between the antenna and therefore the receiver.

[6] High gain amplifiers will enhance the performance of software-defined radio (SDR) receiver systems. SDRs square measure usually designed to be gen- eral purpose and thus the noise figure isn't optimized for anyone explicit application.

[7] Portable electronics devices.

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