High-efficiency class-F Power amplifier with a new design of input matching network

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Abstract: This paper presents a novel access to develop a class-F power amplifier with high power-added efficiency (PAE). The main goal of the proposed PA is to obtain high PAE. The proposed HCC consists a design of output matching circuit (OMN) and input matching combined with a symmetric low-pass filter (LPF) reported. To accomplish a high-efficiency performance, a low-voltage pHEMT in the circuit was executed to supply the required dc-supply voltage. It yielded nth harmonic suppression and high-power added efficiency (PAE). The simulation was carried out using harmonic balance analysis. The power amplifier proposed in this study was fabricated at fundamental frequency of 1 GHz with PAE of 80% and DE of 86% under 12.3dBm input power and very low drain voltage of 2 V. This class-F PA manufactured with such features can be utilized for power amplification in wireless transmitter communication systems.

Key-words: Class-F amplifier, Power added efficiency (PAE), High efficiency, low-pass filter

I. INTRODUCTION

In communication systems, power amplifiers (PA) consume high power; hence, their efficiency is a critical element to be considered in their designing. High efficiency PAs have turned into an important element in modern communications. Radio frequency (RF) power amplifiers are classified into a number of groups like A , B , AB , C , D , E , F , etc. [1-3]. These amplifiers vary in their operation technique, linearity, efficiency, and output power. From among the mentioned classes, owing to its high efficiency and power output, class-F PA has recently become very well-liked

[4-6]. To date, different models have been proposed for modeling PAs, including Volterra series. High efficiency is usually defined as low power use and prolonged battery life [7]. From among several schemes proposed to enhance efficiency, class-F is one of the most appropriate options until now. A class-F PA possesses zero and infinite impedances for even- and odd-order harmonics respectively. It produces square voltage and half sine current wave forms during the transistor drainage [8-9]. Harmonic control circuit is critically involved in the class-F PA design. To design HCC, both lumped and distributed elements can be utilized. Yet, common design methods are complex huge. Thus far, many structures have been proposed to enhance the class-F PAs. Harmonic termination technique (HTT) has been applied to the class-F PA structure [10-11]. In this process, the matching network both transfers the intended impedances and eliminates the undesirable harmonics. In this PA, the highest PAE is 70 %. Harmonic control circuits (HCCs) are developed to produce a high-efficiency class F PA by transmission lines [12]. New HCCs have been confirmed using microstrip resonators [13-15]. As input/output matching networks (IMN/OMN), two microstrip low pass filters (LPFs) are applied, which suppress second tosixth harmonics. Yet, the efficiency is not so high in these works. A microstrip LPF is used in a class-F amplifier to terminate the odd harmonics [16]. This PA is developed at a GHz frequency of 1.1 and has a maximum power-added efficiency (PAE) of 81 %. Doherty PAs with improved efficiency have been extensively

utilized at the back-off region of output power. Yet, because of the quarter-wave transmission lines for loading the impedance modulation, they naturally have a bandwidth restriction [17-22]. To improve the efficiency of a class-F PA by a modified microstrip symmetric LPF, a novel method has been introduced and manufactured. The benefits of the introduced method are presented versus the conventional circuit. With all these characteristics, the proposed PA is a good option for global system.
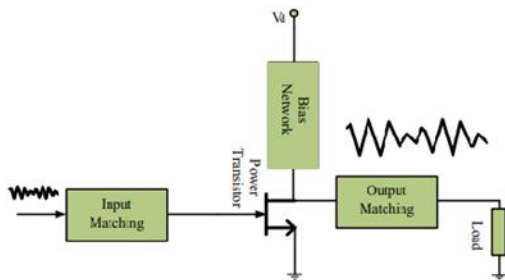

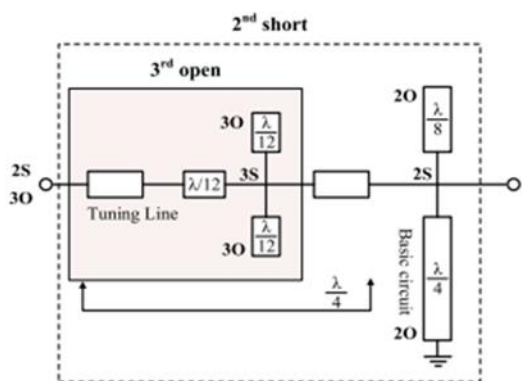Fig. 1. Structure of PAs design

Fig. 2. Harmonic control circuits for class-F amplifier

II. DESIGN PROCESS OF THE POWER AMPLIFIER

A. The basic class-F amplifier

The standard class-F PA mode requires an open-circuit termination at odd harmonic frequencies and short-circuit termination at even harmonic frequencies. This will generate a square voltage waveform and a half-rectified current waveform at its output current-generator plane. These waveforms are described by the following equations [7].

$$V_D(\theta) = V_{DC} + V_m \sin(\theta) + V_{3m} \sin(3\theta) + V_{5m} \sin(5\theta) + \cdots \quad (1)$$

$$i_D(\theta) = I_{DC} - I_m \sin(\theta) - 1_{2m} \sin(2\theta) - I_{4m} \sin(4\theta) + \cdots \quad (2)$$

Where V_{DD} represents drain voltage, I_{DC} shows drain current, and (V m) indicates drain voltage amplitude at the basic frequency. As discussed, the drain voltage includes odd harmonics and the drain current includes even harmonics. In a class-F PA, the power gain and PAE relations are presented as [23] :

$$P_{out} = (V_{DD}^2) \ / \ R \quad (3)$$

$$R = \frac{V_{DD}}{I_{DC}} \quad (4)$$

$$P_{DC} = V_{DC}.I_{DC} \quad (5)$$

$$Gain = \frac{P_{out}}{P_{DC}} \quad (6)$$

$$PAE \quad \frac{P_{out} - P_{in}}{P_{DC}} \quad (7)$$

where R is the load seen by the transistor, P_{out} is the output power use, and P_{DC} is the DC power use. The schematic of a conventional HCC for class-F power amplifiers is shown in Fig.2. In the design process, the second and third harmonics are terminated appropriately to make the circuit simple. We manufactured the output harmonic control networks to control the harmonics. The control circuits include both arm shunt stubs for better harmonic trap and tuning lines for compensating detuning effects of the device's parasitic passive components. Recently, new circuits have been reported that use optical structures [24-33]. These structures are designed using photonic crystals that have high speed and low size[34-40]. Various types of optical amplifiers, optical wall power and various types of logic gates have been reported based on these structures [41-46].

B. Output Impedance and Input Matching at the package plane.

First the fundamental frequency of basic design determined .then the output matching network applied with using the loud pull operation and calculate the equations.
Then the design impedances for the input matching network can be achieved, then for the best performance of parameter the circuit tuned

in advanced design system. A low-pass impedance matching network is used in the proposed PA configuration. For the sake of brevity, a detailed design procedure is presented here. The next section provides the PA configuration and circuit parameters.
for mobile communication (GSM) applications.

Fig. 3 illustrates the basic 1 GHz class-F PA. In this PA, Microstrip stubs are used to develop a traditional HCC block. An advanced design system (ADS) is used to simulate the developed PA, using the RT/Duroid5880 substrate with 2.2 dielectric constant, and 0.381 mm thickness.

In this work, Table 1 presents the VDS = 3 V, VGS = 2.3 V, and other parameters are optimized using an EM-simulator of ADS. . Fig. 4, illustrates the designed class-F PA with the output power, gain, and efficiency. As indicated, the highest PAE is 63% and the highest gain is 12.93dBm.
The simulated voltage (Vm) and drain current (Im) waveforms, which are approximates of square and half sin waveforms respectively, are shown in Fig. 5.

Fig. 4, Simulated gain zand PAE of basic PA

Fig.5, Simulated drain voltage and drain current waveforms

C. Input Matching

Based on the output matching network implemented, the optimal impedances for the input matching network can be obtained .In the proposed PA configuration a low–pass impedance matching network is utilized. The detailed design procedure is shown here for brevity. Its configuration and circuit parameters will be given in the next section.
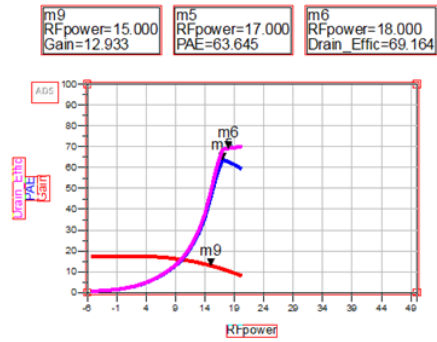

Fig. 3. The basic class-F PA design

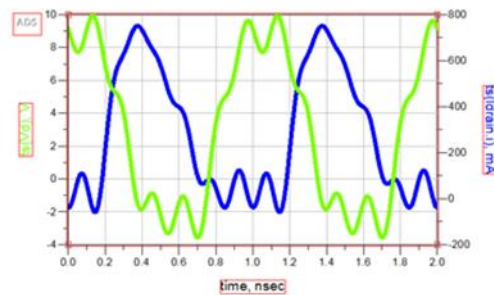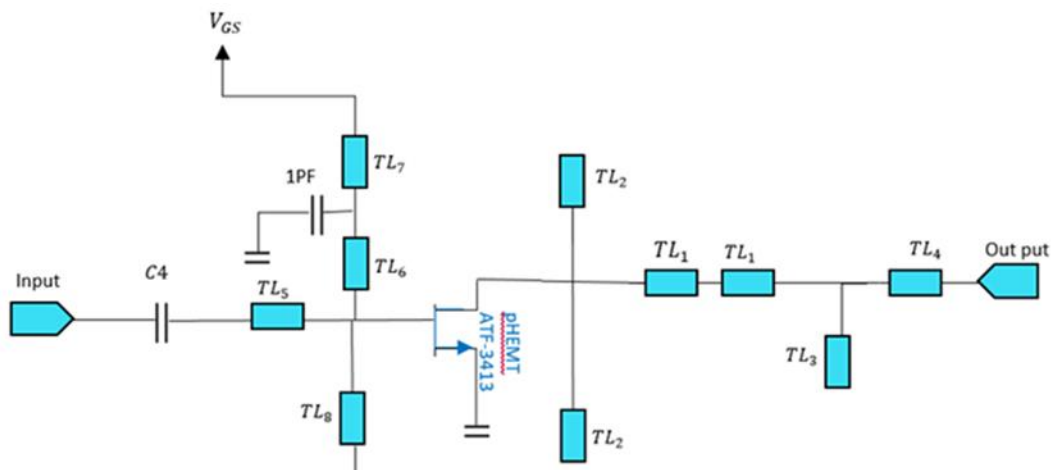Table 1. Stub dimensions applied in the class-F PA introduced

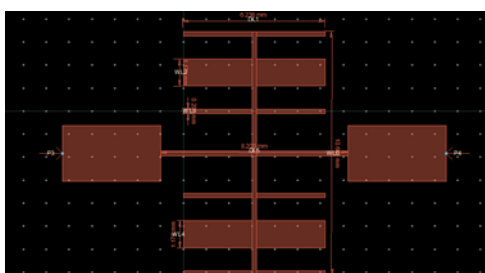| Stubs name	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9
Length (mm)	2.67	29.1	2.7	9.5	9.5	1.5	7.75	28.3	2.5
Width (mm)	1.56	9	2.4	1.6	1.6	2.67	1.53	5	0.625

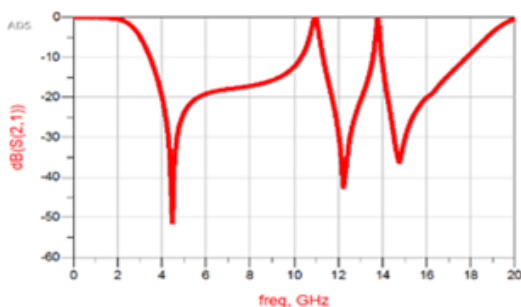Fig. 6, The structure of MMR

Fig. 7. S21 parameters of MMR.

III. NEW DESIGN APPROACH NOVEL HCC DESIGN

The major microstrip resonator (MMR) is used in the HCC design process to match the intended impedances with PA input and to remove the excessive harmonics (Fig. 6). Usin the mentioned substrate, the designed MMR is simulated with the ADS simulator. The dimensions of the principal microstrip resonator (MMR) include: $DL_1 = 6.2$ mm, $WL_2 = 1.178$mm, $WL_3 = 0.2$ mm, $WL_4 = 1.178$ mm, $DL_5 = 8.2$ mm, $WL_6 = 10.6$ mm. The introduced resonator is of a symmetric shape (Fig. 6), so it is predicted to show a reciprocal response.

The resonator is designed with a cut-off frequency of -3dB. This frequency is larger than the fundamental frequency of the suggested PA. The simulated S-parameters of the introduced resonator are shown in Fig.7. The resonator has a cut-off frequency of -3dB at 5.6 GHz in the passband. It has a low insertion loss in the passband but has a narrow stopband bandwidth and gradual transition band. To enhance the proposed expanded prototype elliptic function resonator. The overall dimensions of the designed MMR are 8.2 mm-× 10.6 mm.
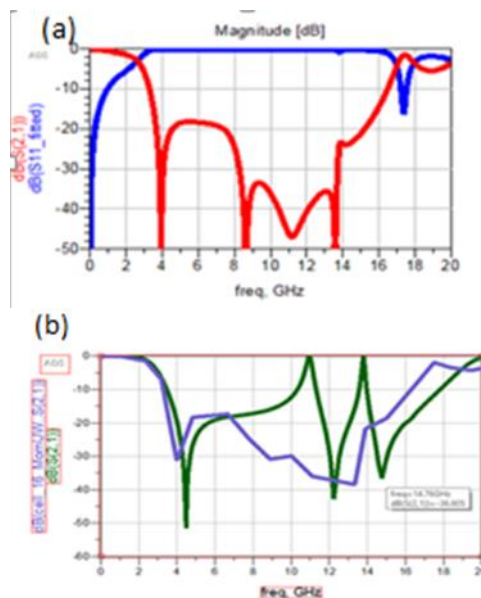

Fig 9.a Simulated S21 & S11 parameters of this LPF, Fig.9.b Shows comparison between S21 parameter of MLPF&MMR
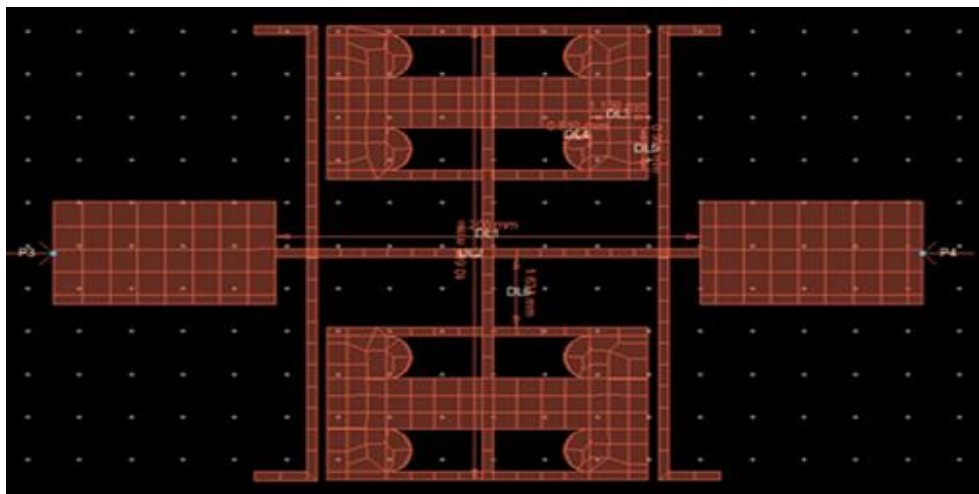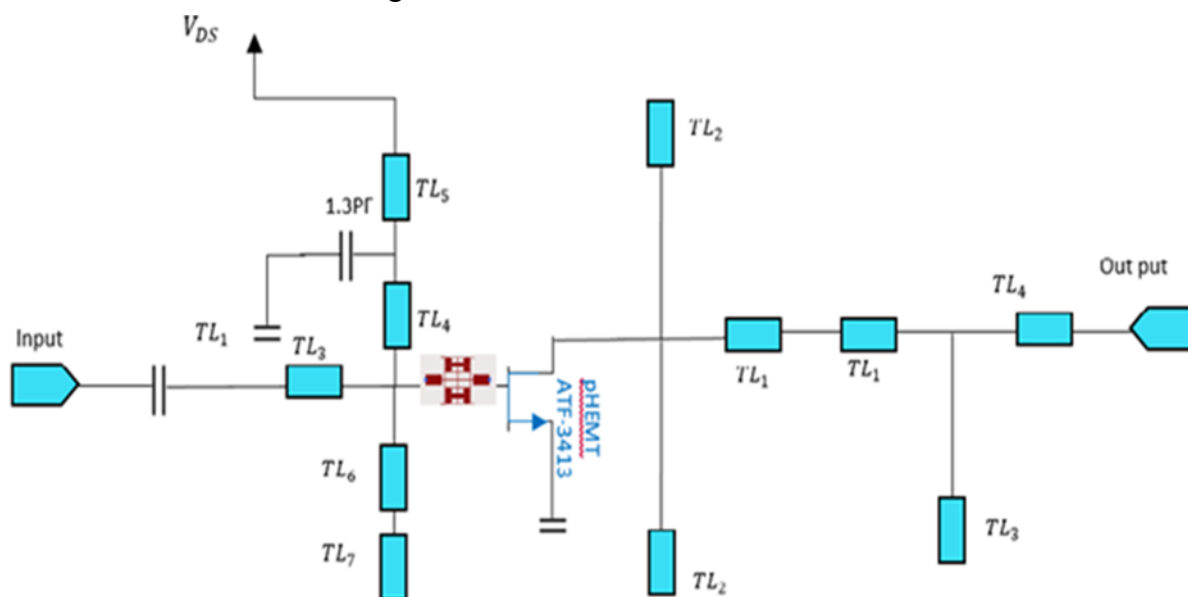
Fig.8 The structure of this LPF

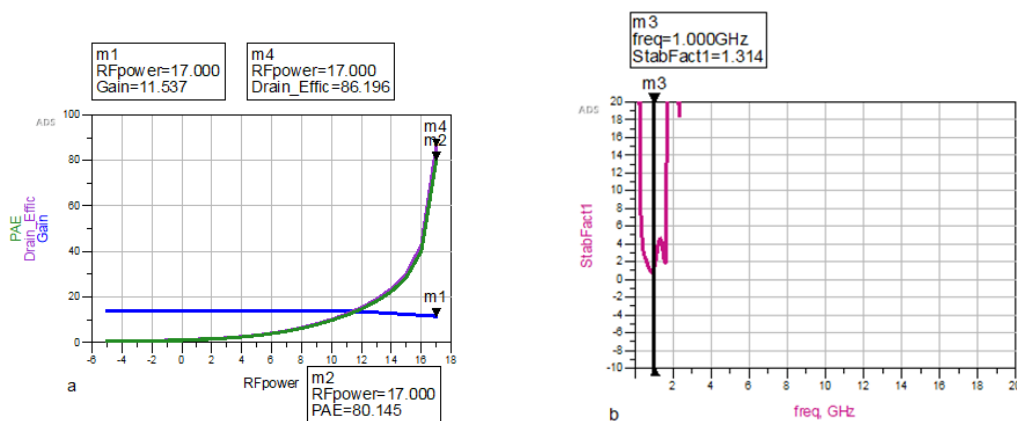Fig. 10. The schematic of the proposed   PA

Fig. 11(a) Simulated PAE, power gain and DE of the proposed amplifier with LPF,

(b), the stability factor of this PA

As seen in Fig. 11, the maximum PAE value of a proposed class-F PA is 80% at the 1GHz operating frequency and the maximum power gain of this amplifier is equal to 11.537dB, the stability factor of this power amplifier in 1 GHz is about 1.34.
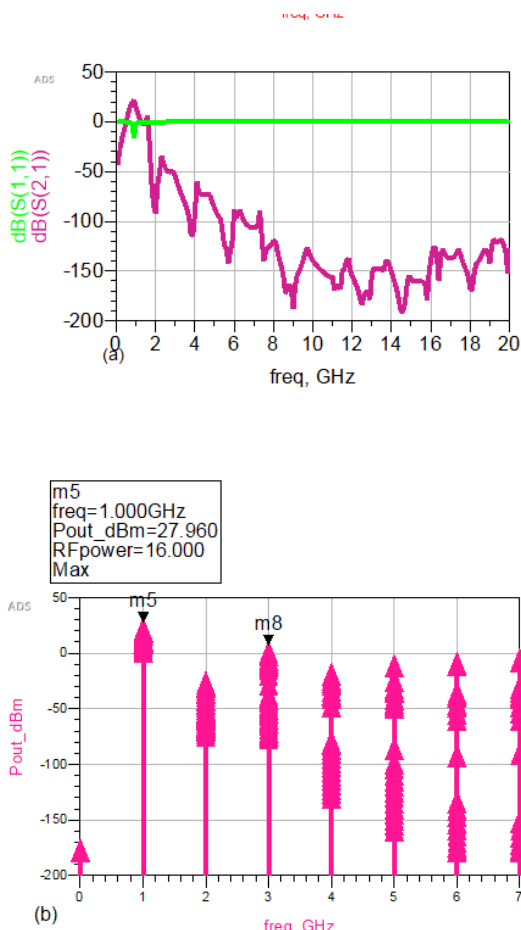

Fig. 12 (a) simulation S(21) and S(11) parameter of this Class-F PA,(b) Output power at fundamental frequency and other seventh harmonics

F power amplifier has good performances such as, high efficiency compared to the other works. Thesimulation and measurement have been performed using ADS software and Agilent technology CXA-N9000A signal analyzer, respectively. In this design pHEMT

The output power of the proposed class-F amplifier with LPF at fundamental frequency and 7th harmonics is shown in Fig.12(b), which shows acceptable linearity region of the PA at operating frequency.

Table 2 shows performance compression of proposed class-F amplifier and various related class-F PAs. Important parameters such as: power added efficiency (PAE), the output power (Pout), are listed in this table. Amplifiers with GaAs transistors are consumed more power and feature more efficiency. Amplifiers with pHEMT transistors have rather lower powerIn the proposed design, at first, a pHEMT transistor is used. The results show that the efficiency parameter is improved in the final proposed amplifier by using a novel HCC block. The results illustrate that the proposed class F power amplifier has good performances such as, high efficiency compared to the other works. The simulation and measurement have been consumption and lower efficiency.

proposed amplifier by using a novel HCC block. The results illustrate that the proposed class

ATF-34143 transistor is used class -F amplifier. Fig. 13 shows, comparison between proposed class-F PA with LPF and primitive PA without LPF.

This figure clearly illustrates the superior of the proposed amplifier in comparison of the primitive PA .The drain and gate of the transistor are fixed at 3 V and -0.75 V, respectively. The designed class-F PA is fabricated on an RT/Duroid5880 with relative permittivity of ε_r =2.2 and a thickness of 0.381 mm. The photograph of fabricated PA shown in Figure.14.The proposed class-F PA occupies an area of 65 × 70 mm².It is evident that the proposed PA has high efficiency and output power with proper supply voltage and circuit area. Also, the PAE, Pout and Gain performance, the proposed amplifier is a narrow band and it operating frequency is 1GHz.

Table 2. comparison with other works

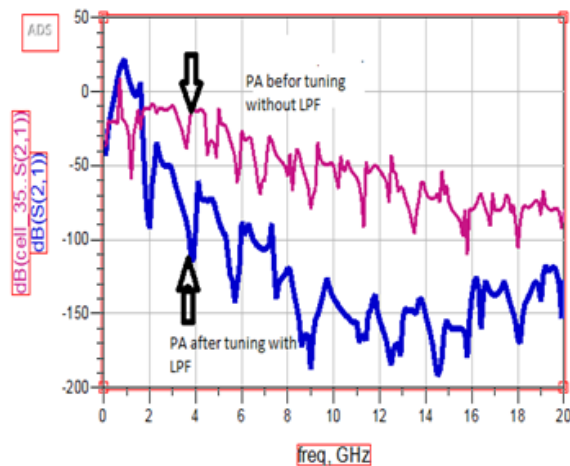| Refs.	year	Freq. (GHz)	PAE	Pout	Device	Gain	Drain efficency	Pdc
[1]	2020	1.25	60.4%	29	GaAs	17.9	65.2	Class F
[2]	2019	1.8	75%	28	GaAs pHEMT	-------	-------	Class F
[6]	2006	1	64%	22.5	GaAs MES FET	12		Class F
[7]	2018	0.5-2.3	52-80	39.2	GaAs pHEMT	11.7	60-81	Extended continuous Class-F
[12]	2019	0.9	74%	29	GaAs pHEMT	18.5		Class F
[16]	2019	2.4	83%	23.6	GaAs pHEMT	10		Class- F
This work		1	80%	17	GaAs pHEMT	11.5	86	Class- F

Fig. 13 comparison between proposed class-F PA with LPF and PA without LPF

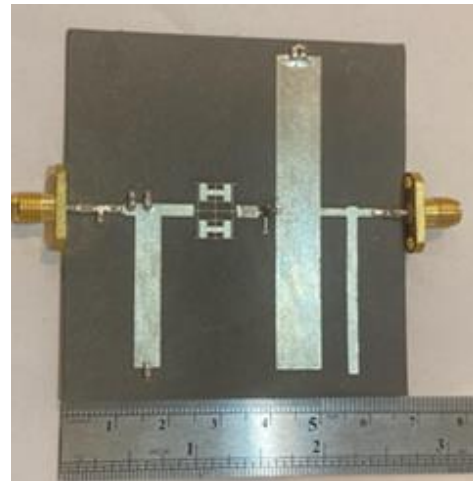
Fig.14, photograph of fabricated PA

IV. CONCLUSION

A new design introduced for a high- efficiency PA is utilized to suppress the unwanted harmonics and reduce the parasitic effects of the element. For the validation of the proposed design, a class-F PA has been fabricated at fundamental frequency of 1 GHz and using an ATF-34143 transistor, a new elliptic-function LPF was added to input matching network amount results show that PAE and DE values are 80% and 86%, the output power greater than 28.29dBm.

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